Ph. D. Thesis
박사 학위논문

Ultra-low Power Receivers Based on Injection Locked Oscillators

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A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Information and Communication Engineering. The study was conducted in accordance with Code of Research Ethics[1]

11. 06. 2020

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Ultra-low Power Receiver Based on Injection Locked Oscillators

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ABSTRACT

This thesis presents an ultra-low-power receiver based on the injection-locked oscillator (ILO), which is compatible with multiple modulation schemes such as on-off keying (OOK), binary frequency-shift keying (BFSK), and differential binary phase-shift keying (DBPSK). The receiver has been fabricated in 0.18 μm CMOS technology and operates in the ISM band of 2.4 GHz. A simple envelope detection can be used even for the demodulation of BFSK and DBPSK signals due to the conversion capability of the ILO from the frequency and phase to the amplitude. In the proposed receiver, a Q-enhanced single-ended-to-differential amplifier is employed to provide high-gain amplification as well as narrow band-pass filtering, which improves the sensitivity and selectivity of the receiver. In addition, a gain-control loop is formed in the receiver to maintain constant lock range and hence frequency-to-amplitude conversion ratio for the varying power of the BFSK-modulated receiver input signal. The receiver achieves the sensitivity of –87, –85, and –82 dBm for the OOK, BFSK, and DBPSK signals respectively at the data rate of 50 kbps and the BER lower than 0.1 % while consuming the power of 324 μW in total

This thesis presents an ultra-low power, low cost demodulator for gaussian frequency shift keying (GFSK) receivers that use low intermediate frequencies (IF). The demodulator employs a direct IF to digital data conversion scheme by using an injection-locked ring oscillator (ILRO) with a 1-bit flip-flop. It consumes 2.7 μW from a 1.0 V supply at a data rate of 500 kbps achieving an energy efficiency of 5.4 pJ/bit which is 30 times better than that of the recently presented works. The demodulator also achieves 17.5 dB SNR at 0.1 % BER while operating at the same date rate. The demodulator is implemented in a 0.18 μm standard CMOS process and occupies an active area of 0.012 mm^2.

Keywords: Ultra-low power, injection-locked oscillator, injection-locking receiver, multi-modulation, frequency-to-amplitude conversion, phase-to-amplitude conversion, wireless sensor node, internet of things, single-ended-to-differential conversion, *Q* enhancement, envelope detection, Demodulator, GFSK, low power, low-IF, CMOS.

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I. INTRODUCTION

1.1 Motivation

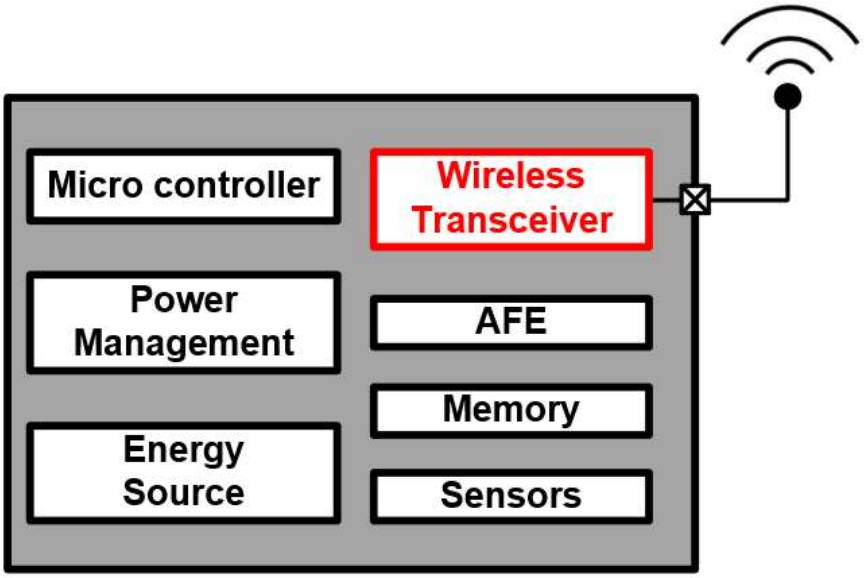


Figure 1.1 Conceptual block diagram of wireless sensor node for IoT.

As a variety of services and applications based on the internet of things (IoT) have been widely developed, the demands on ultra-low power (ULP) wireless techniques for data transmission and reception have grown rapidly. The capability of performing wireless communication with little power consumption is a key factor enabling the operation of ubiquitous sensor nodes (USN) for IoT [1]. As the complexity and scale of the IoT system increases and the number of sensor nodes in the network becomes large, connecting the sensor nodes to the power lines makes the installation of the system prohibitively expensive if not impossible. It is therefore preferred to power the sensor nodes by batteries. In such battery-powered sensor nodes, low power consumption is an essential requirement considering that the power consumption of the sensor node determines the replacement or

recharging frequency of the battery and directly affects the maintenance cost of the IoT system.

Furthermore, to realize the vision of the hyper-connected world filled with trillions of sensor nodes, researchers are working toward the energy-autonomous operation of the wireless sensor nodes, which are powered by the energy harvested from their ambience. In this scenario, the average power consumption of the overall sensor node must be lower than the average rate of energy harvesting. It poses extreme limitations on the power budget of the wireless sensor node, even if the duty-cycled operation scheme is employed to cut down the amount of the power dissipated on average. Since the wireless transceiver is the most power-hungry block in the typical wireless sensor node as shown in Fig. 1.1, reducing the power consumed for wireless communication is critical.

On the other hand, the choice of modulation scheme has a significant impact on the transceiver design in various aspects such as power consumption, complexity, performance, and reliability. For short-range low-power communication, the transceivers based on on-off keying (OOK) have been widely implemented. The OOK modulation scheme allows achieving very low power consumption because of the simple circuit architecture used for the transceiver design. For example, the demodulation function of the receiver can be implemented by using an envelope detector without requiring any high-power-consuming circuit components such as oscillators, mixers, and frequency synthesizers [2]–[4]. However, the OOK receiver based on such a simple structure has low sensitivity and high susceptibility to the interferers compared to the receivers employing other modulation schemes such as frequency-shift keying (FSK) and phase-shift keying (PSK). To overcome the limited sensitivity performance, a high-gain amplifier and an expensive external

filter are required to precede the envelope detector [2]. The FSK modulation with a constant envelope, on the other hand, enables the use of an energy-efficient nonlinear power amplifier in the transmitter. However, the receiver requires the precise local oscillator and quadrature signal paths, which results in a complex receiver structure consuming relatively high power.

Hence, it is essential to investigate ULP wireless receiver used in wireless sensor node for IoT while overcoming the limitation of the receiver performance according to modulation schemes. In this thesis, the ULP wireless receiver which can support multiple modulation schemes and ultra-low power Gaussian FSK (GFSK) demodulator based on a signal conversion scheme of an injection locking technic are proposed and demonstrated.

1.2 Design Consideration of Receiver for Internet of Things

Generally, the requirements of receiver depend on the application of interest. In wireless sensor node for IoT applications, battery life, capacity, communication distance and compatibility should be key considerations as well. For the realization of wireless sensor nodes used in IoT, the implementation of receivers used in each sensor node should optimize the following four characteristics.

- Low Power Consumption: The Power consumption determines the size of the battery installed or integrated and the lifetime of the sensor node. Mechanisms to reduce power consumption improve the lifetime of the wireless sensor node
- High Sensitivity: The sensitivity of receiver in sensor node is related to the power consumption of transmitter and communication distance.
- High Channel Selectivity: The higher channel selectivity of the receiver can form many channels between numerous sensor node within the assigned frequency band.
- High Compatibility with Wireless Standards: The use of wireless standards can improve compatibility between wireless sensor node and other wireless devices.

A wireless transceiver is the most power-hungry block in the sensor node as mentioned above. If the power consumption of the components consist of the transceiver is minimized, the sensor node used for IoT can extend the lifetime or reduce the size of the battery. Therefore, in order to improve the lifetime of the sensor node used for IoT, the low power design should be the top priority.

Secondly, if the sensitivity of receiver in the sensor node is improved, the transmission power of the transmitter can be reduced. Thereby, the transmitter consumes relatively low power. That results in an extended communication range consuming same power.

In the receivers used in IoT application, each sensor node forms a network and communicates with each other. So, a high channel selectivity is required for multi-channel operation.

In order to use the existing well-defined communication network, a communication between wireless devices and sensor node is possible by using a suitable wireless standard. For example, Currently, wireless communication standards such as Bluetooth using FSK, Zig-bee using PSK, and RFID using ASK are typical.

The injection locked oscillator (ILO) in the proposed receiver in this thesis allows to use of a simple envelope detection circuit which can reduce total power consumption of receiver. Also, the Q-enhanced single-ended-to-differential amplifier (SDA) is employed to provide high sensitivity and high selectivity. Furthermore, the proposed receiver is suitable for a variety of modulation schemes such as OOK, FSK, PSK by using signal conversion characteristic of ILO.

1.3 Conventional Architecture

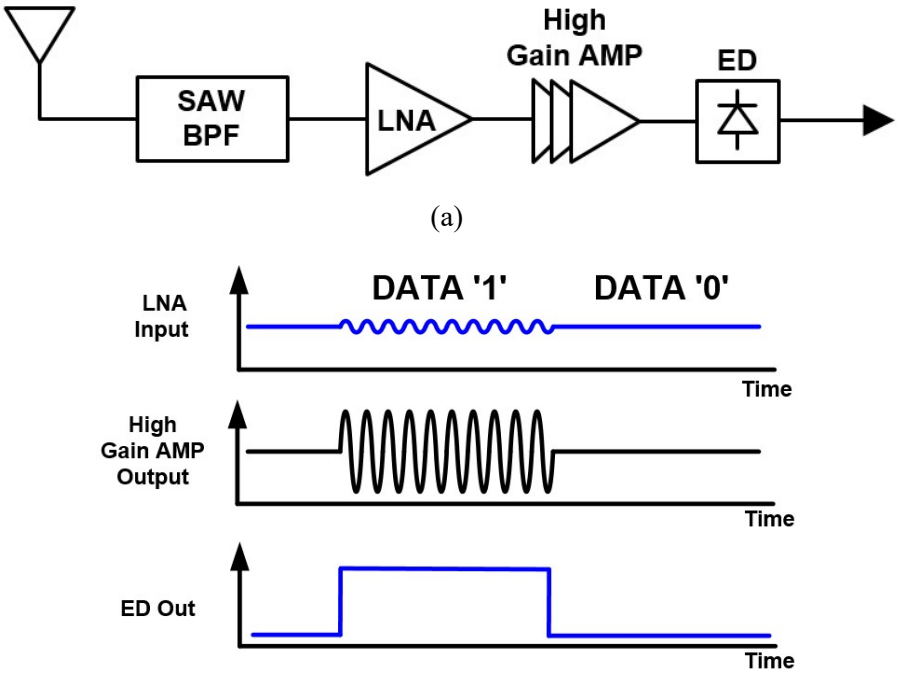


Figure 1.2 Tuned-RF receiver (a) block diagram (b) operation.

Recently, to overcome the limitations of the conventional receivers, a variety of new receiver structures for ultra-low power (ULP) consumption have been introduced. However, most of the developed receivers have several drawbacks to use in the IoT network mentioned above. Most of the recent low-power receivers employ an envelope detection architecture with OOK modulation because of its simplicity which leads to the best power efficiency.

The tuned-RF architecture which has a very simple structure is shown in Fig. 1.2 (a). The received input signal should be amplified before applying envelope detector (ED) to improve the sensitivity of the receiver. Achieving such amplification at minimal power consumption has been the main design target of the recently proposed architectures. However,

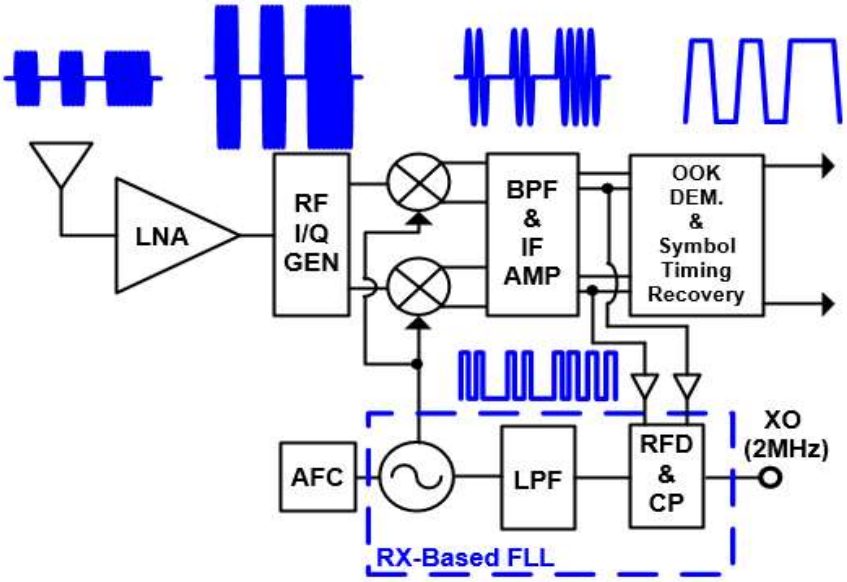
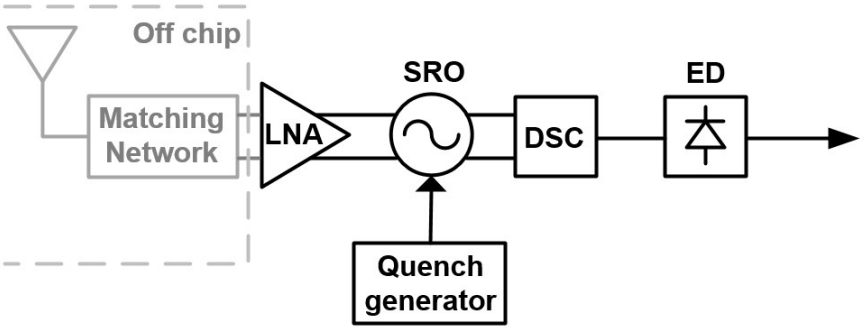


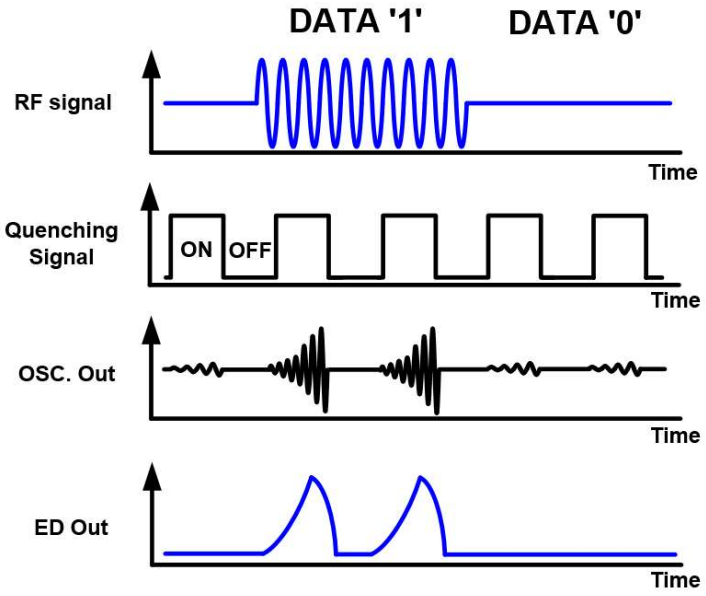
Figure 1.3 Low-IF receiver.

the front-end amplifier in the tuned RF architecture [2] consumes significantly larger power due to operating in the high frequency. Therefore, there is a limitation to achieve the high sensitivity in the given power budget. Additionally, to achieve the high selectivity, an external, discrete High-Q SAW filter is required. Such filters occupy a very large size and hence they increase the size and cost of the receiver.

Another conventional architecture is Low-IF. Fig. 1.3 shows the low-IF receiver structure, where the receive path itself operates as a part of the frequency-locked loop (FLL) for LO generation [5]. The Low-IF receiver architecture is resilient to DC offset and 1/f noise in comparison with a Zero-IF receiver architecture. Since the mixers in the receive path perform frequency down-conversion for not only receiver function but also FLL operation, the high-precision LO signal can be generated without using a power-hungry frequency divider. However, the structural complexity is high due to the FLL and quadrature demodulation circuits.



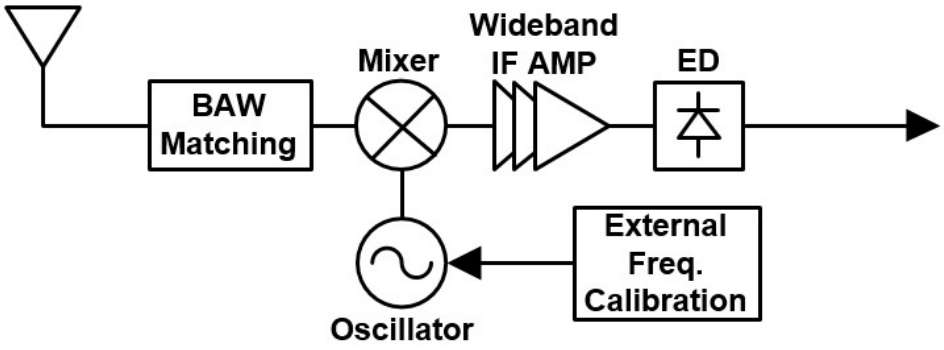
(a)



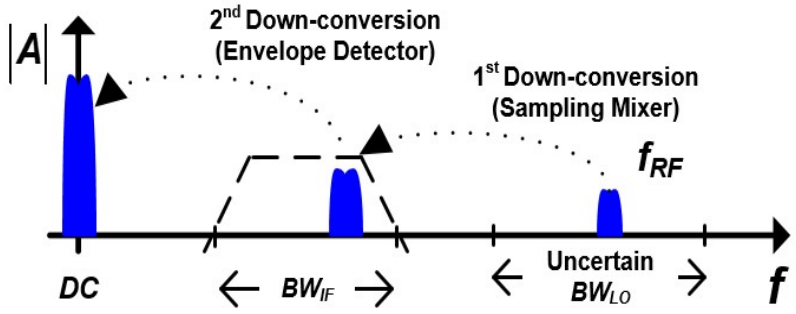
(b)

Figure 1.4 Super-regenerative receiver (a) block diagram (b) operation.

The super-regenerative receiver is not commonly used as super- heterodyne or direct conversion receiver architecture due to the low selectivity. Recently, however, due to its simple structure and low power consumption, the super-regenerative receiver is used in local area communication. Fig. 1.4(a) shows the receiver structure of the super-regenerative receiver for OOK modulation [6]. The output of the receiver is determined using a quenching signal and RF signal input to the super-regenerative oscillator (SRO).



(a)



(b)

Figure 1.5 Uncertain-IF receiver (a)block diagram (b)operation.

The operation of super-regenerative receiver is shown in Fig. 1.4(b). In accordance with the low frequency quenching signal, the super-regenerative oscillator is operated in an oscillating mode (quenching signal is high) or damping mode (quenching signal is low). When the RF signal with large amplitude is applied through the antenna and quenching signal is high, the output amplitude of the oscillator will very rapidly reach a steady state. Then, the output of ED goes high level. On the contrary, if the RF signal amplitude is low and quenching signal is high, the output amplitude of the oscillator cannot reaches a steady state. As a result, there is no change in the output of ED. Even though the RF signal with in the vicinity of free running frequency is applied to the SRO, the SRO makes steady state output signal. Therefore, the selectivity of this receiver is poor.

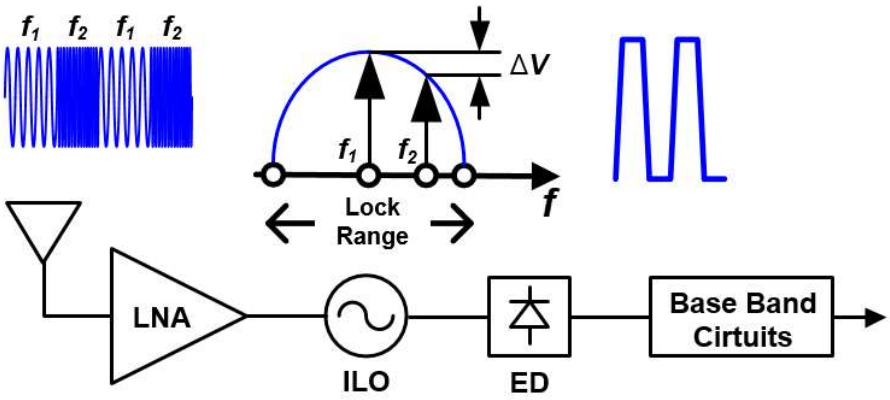


Figure 1.6 Injection locking receiver.

Fig. 1.5 shows the structure of the uncertain-IF receivers [7]. In this structure, a low- power free-running ring oscillator is used to generate the local oscillator (LO) signal for down-conversion. Due to the inherent uncertainty of the LO signal frequency, the IF frequency is not clearly determined, and the selectivity performance of the receiver is therefore low.

Fig. 1.6 shows the receiver structure based on the injection-locked oscillator [8], [9]. The ILO plays an essential role of converting the frequency-modulated signal to the amplitude-modulated signal, which enables the energy-efficient implementation of the FSK receiver. The amplitude-modulated signal generated by the ILO is down-converted by the envelope detector as in the conventional low-power OOK receiver. This structure, however, faces significant challenges in that the amplitude of the signal injected to the ILO should be sufficiently large for guaranteeing proper injection-locking operation and kept relatively constant for maintaining consistent frequency-to-amplitude conversion ratio.

The receiver characteristics of the five recently published structure are summarized in Table 1.1 The tuned-RF and the uncertain-IF architecture has high selectivity due to the external High-Q filter. Even the Low-IF architecture has high complexity and low sensi-tivity, it reduces power consumption significantly using RX-path in a frequency

Table1.1 Comparison of characteristics of receiver architecture

	Tuned-RF	Low-IF	Uncertain- IF	Super Regenerative	Injection Locking
Power	Low	Low	Low	Low	High
Sensitivity	Low	High	Low	Low	Low
Selectivity	High	Low	High	Low	Low
Simplicity	Simple	Complex	Simple	Simple	Simple
Modulation	OOK	OOK	OOK	OOK	FSK

locked loop circuit. The uncertain-IF receiver architecture is possible to reduce power consumption because it does not need an accurate, high quality local oscillator.

The super-regenerative receiver can reduce power consumption because of its simplicity. However, the selectivity and sensitivity is low due to the inherent characteristics of SRO. The injection-locking receiver consume a high-power. Because the high gain is required in front of ILO for the injection locking. Nevertheless, this receiver has an advantage that is robust against to the interferer compare with other receivers due to using a FSK modulation.

1.4 Proposed Structure

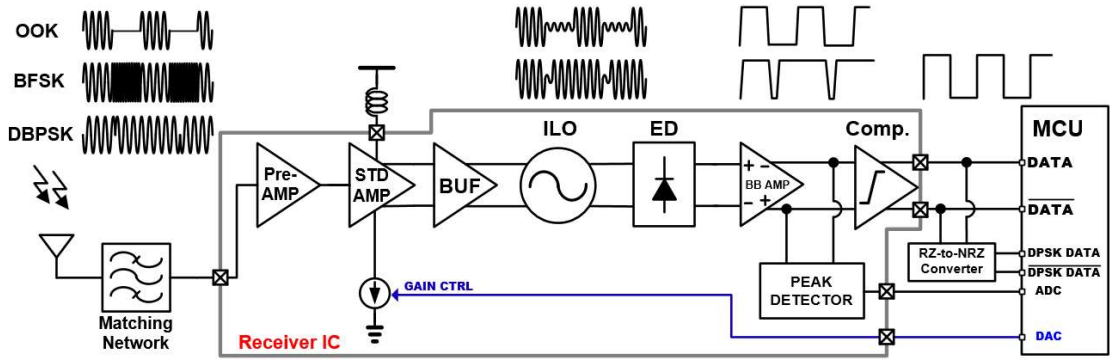


Figure 1.7 Overall architecture of the proposed wireless receiver system.

The block diagram of the proposed receiver is shown in Fig.1.7. The proposed receiver consist of the front-end matching network, RF receiver IC, and microcontroller unit (MCU). The pre-amplifier connected to the antenna through a matching network amplifies the RF signal. The Pre-AMP amplifies the RF signal with moderate gain and provides isolation between the matching network and the single-to-differential amplifier (SDA) input. The STD significantly improves the sensitivity of the overall receiver system by using Q-enhancement. The *Q*-enhancement technique is applied to the SDA so that high gain can be achieved over a narrow frequency band. The narrow band filtering effect provide high selectivity. In addition, the STD converts its single-ended input signal to differential signal that drives the injection locked LC oscillator.

The output amplitude of the ILO changes depending on modulation scheme such as Fig. 1.8. For the OOK input signal as shown in Fig. 1.8 (a), the ILO simply adds the constant amount of signal amplitude as explained in Chapter II, and thus the amplitude variations of the input signal are preserved at the ILO output.

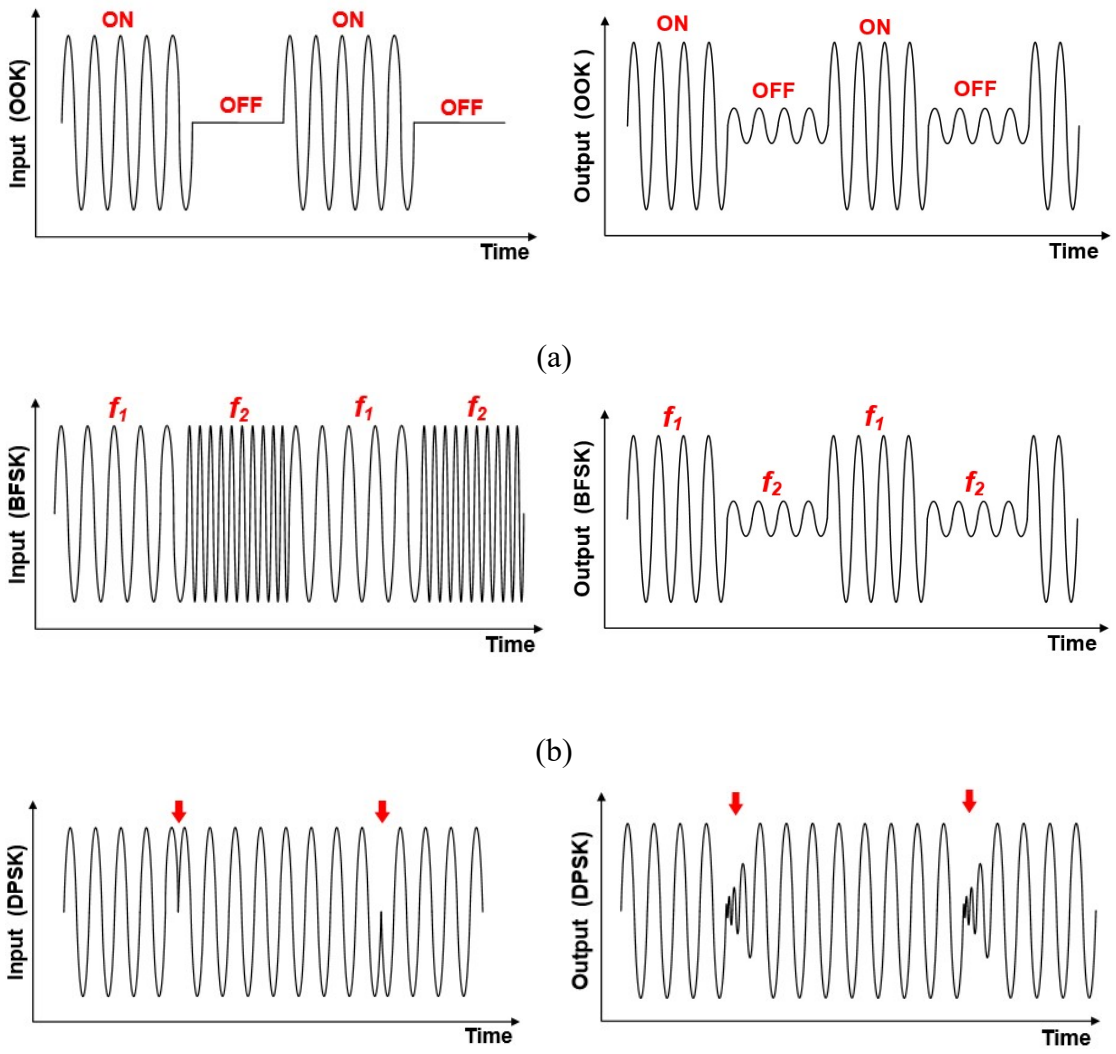


Figure 1.8 Input and output waveform of (a)OOK (b)BFSK (c)DPSK.

The BFSK signal as shown in Fig. 1.8 (b), ILO output has a large amplitude when the frequency of the injection signal (ω_1) is close to the free-running frequency of the ILO (ω_0), while the output amplitude becomes small when ω_2 is far from ω_0 as shown in Fig. 1.8 (b). In DPSK scheme such as Fig. 1.8 (c), the output amplitude is fluctuated such when the phase of injection current is shifted 180˚.

Table 1.2 Target Specification of Proposed Receiver System

Item	Design goal	Unit
Operating Frequency	2.4 GHz ISM band	-
Modulation	FSK(or OOK, PSK)	-
Data Rate	≥ 10	Kb/s
Sensitivity	< -85	dBm
power consumption	< 350	μW

Hence, The ILO not only translates the OOK/BFSK/DBPSK signal to the amplitude-modulated signal but also improves the receiver sensitivity because the weak RF signal injected to the ILO generates the oscillator output signal having a relatively large swing.

The ILO output is down converted to a baseband signal by the envelope detector. The baseband signal is further amplified by a BB AMP. The BB AMP output is compared with a threshold of comparator and it generate the final data output.

The lock range of the ILO changes due to the varying magnitude of the injection signal, the frequency-to-amplitude conversion ratio doesn't stay constant. To keep constant lock range of ILO, input signal amplitude should be kept constant. So Peak detector capture output amplitude of BB AMP and amplitude information send to ADC of external MCU and DAC Block control the gain of STD. The target specification of proposed receiver system are summarized in Table 1.2.

1.5 Overview of this Thesis

This thesis demonstrates a multi-mode ultra-low power receiver based on an ILO which achieves the high sensitivity and channel selectivity. These properties are provided by modulation conversion property of ILO, the Q-enhancement of SDA and auto gain control loop. In this thesis, a GFSK demodulator is also demonstrated using ILO. The frequency to phase conversion process of ILO is possible to use simple structure and to operate with ultra-low power. In chapter 1, the brief introduction of thesis is described. The preceding chapter provide the properties of conventional architectures and the overall architecture of the multi-mode ultra-low power receiver based on an ILO.

Chapter II focuses on the operating principle of ILO with LC and Ring type. Moreover, the detail of signal conversion process in the lock state of ILO is explained.

Chapter III introduces a multi-mode ultra-low power receiver based on an ILO which exploits the properties of ILO. This chapter include the detail of a low-power receiver design based on ILO, which can support multiple modulation schemes: OOK, binary FSK (BFSK), and differential binary PSK (DBPSK). A Q-enhanced SDA is employed to provide high gain and generate the injection signal with sufficient strength. Moreover, the consistency of the receiver performance is greatly improved by controlling the amplitude of the injection signal in a closed-loop manner.

The GFSK demodulator for low-IF receivers presented in in Chapter IV. This chapter presents the detail of the proposed demodulator architecture employing an ILO. Due to the frequency to phase conversion property, The proposed demodulator is able to use simple structure which consist of limiter, pulse slicer, ILO and D-flip flop. The simulation and chip measurement results of proposed demodulator explained this chapter. Then, the conclusion and further studies introduced in Chapter V.

II. INJENTION LOCKED OSCILLATOR

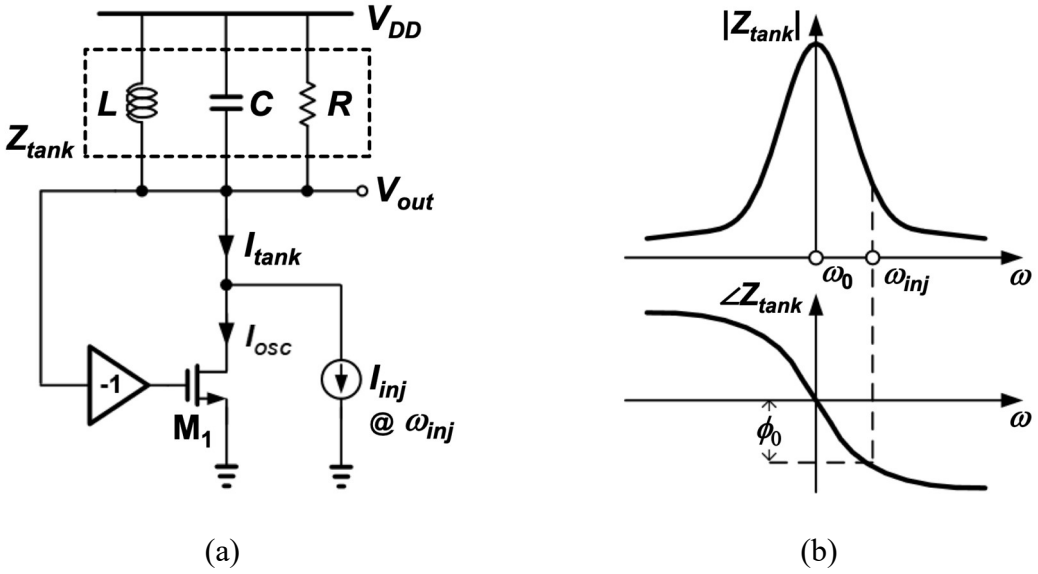
When two systems with independent output frequencies are in close contact, the interaction between two systems can change the operating frequency of the two systems. Using two frequencies that are very close, but slightly different, the mutual influence can cause the two systems output one specific frequency. This phenomenon is called injection locking. However, the deviation between the two output frequencies is too large, injection pulling which the output signals pull each other in the frequency domain can occur. In this case, the output of the two systems varies in time domain. The frequency range for injection locking is defined as the lock range, and the two output signals are out of this range, injection pulling occurs.

Injection pulling is always considered an undesirable phenomenon because the output frequency of system changes over time. On the other hand, injection locking can be very useful in some applications. For example, there is a very low-noise signal with a well-defined output frequency, the stable oscillator output is obtained through inject locking by using this signal.

In this chapter, through a mathematical approach, the basic operation principle of the ILO according to the oscillator structure is presented. Mathematical equations are applied to the injection locking and pulling have been made and based on a study of Adler [10], Razavi [11]. Subsection 2.2 describes the conversion process between the injection signal and the output signal of the oscillator in the injection locking state.

2.1 Operating Principle

2.1.1 Injection Locked LC Oscillator



(a) (b)

Figure 2.1 (a) Conceptual diagram of ILO, and (b) freuquency response of LC tank.

When the Injection signal has similar frequency to the oscillation frequency (resonance frequency of the LC Tank) is injected into oscillator, the output signal is synchronized to Injection signal. Hence, the frequency of output signal becomes same frequency with injection signal. The operation of injection-locked LC oscillator is described in Fig. 2.1. Fig. 2.1 (a) shows the conceptual diagram of the injection-locked LC oscillator. In the injection-locked LC oscillator, for the oscillation to sustain, the total phase shift of the loop ($\angle H$) must be a multiple of 2π and magnitude of loop gain ($|H|$) must be larger than 1, as to meet the Barkhausen criteria [11]. In Fig. 2.1 (a), $|H|$ and $\angle H$ can be described as follow:

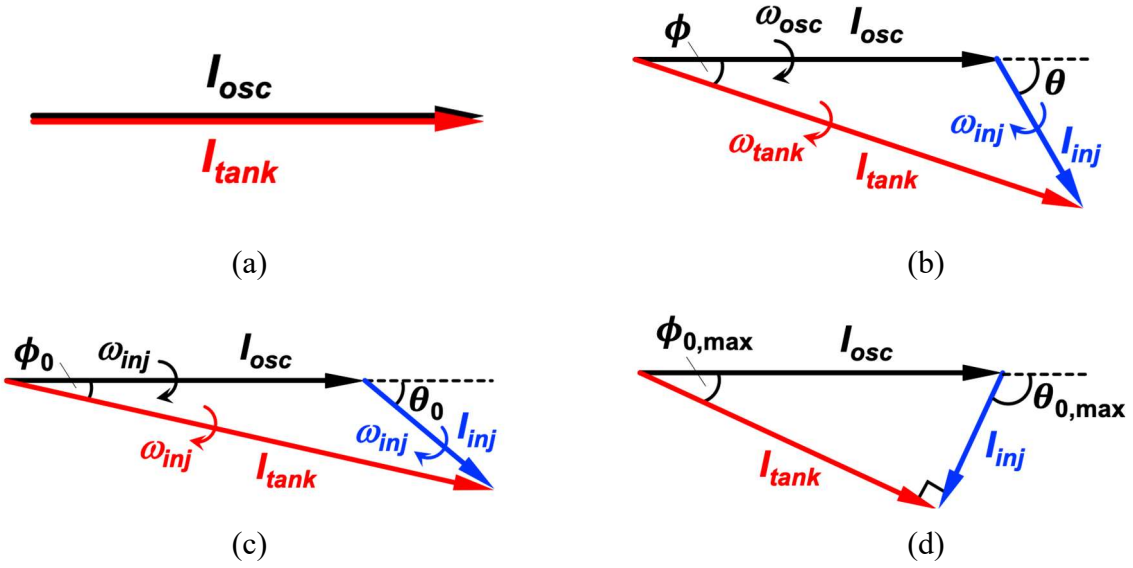


Figure 2.2 Phasor diagrams of ILO currents when the ILO (a) runs freely, (b) experiences locking transition, (c) is locked, and (d) operates at the edge of its lock range.

$$|\mathrm{H}(\mathrm{s}=\mathrm{j}\omega_0)| = g_m R \geq 1 \tag{2.1}$$

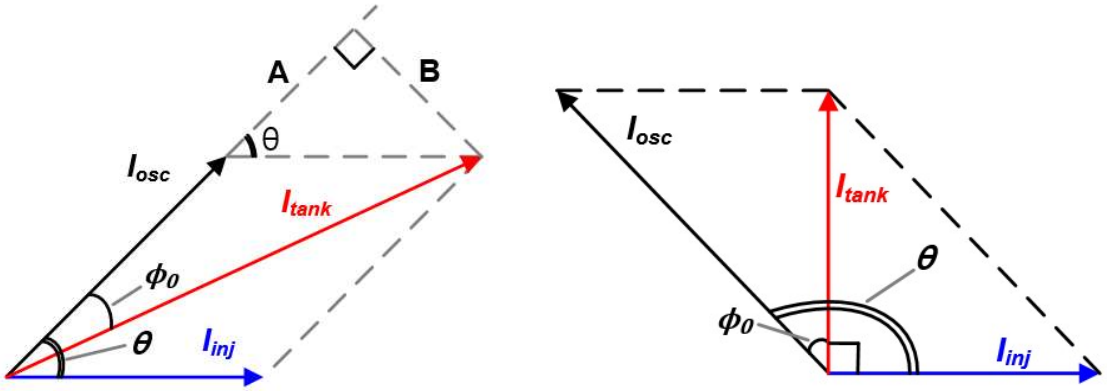
$$\angle H(s = j\omega_0) = 360° \tag{2.2}$$

At ω_0, the Z_{tank} contributes no phase shift, as illustrated in Fig. 2.1 (b), while the inverting buffer and M_1 create a total phase shift of 360°. The oscillation frequency is defined by [12],

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{2.3}$$

In the free-running condition, the magnitude and phase of I_{tank} are the same as those of I_{osc}, as shown in Fig. 2.2 (a).

Now assume that the injection current I_{inj} having the frequency of ω_{inj} is applied to the ILO. Since the I_{tank} should be the vector sum of I_{osc} and I_{inj}, the relationship among I_{osc},



(a) (b)

Figure 2.3 Phase diagrams of the different currents (a) Arbitrary ϕ_0 (b) $\phi_{0,max}$.

I_{inj}, and I_{tank} can be described by the phasor diagram as in Fig. 2.2 (b). Before locking, the phasors, I_{osc}, I_{inj}, and I_{tank} rotates clockwise with different angular velocities, ω_{osc}, ω_{inj}, and ω_{tank}, respectively. Hence, the angle θ between I_{osc} and I_{inj}, as well as the angle ϕ between I_{osc} and I_{tank}, varies over time. After this transition process, if I_{inj} is not too small and ω_{inj} is not too far from ω_0 to achieve injection-locking, the angle between the I_{osc} and I_{tank} becomes ϕ_0, as shown in Fig. 2.2 (c), and this phase difference is compensated by the phase shift of Z_{tank}, as described in Fig. 2.1 (b). It makes the total phase shift around the feedback loop become 360°, and thus the ILO locked to the injection signal. Once injection-locked, the phasors I_{osc}, I_{inj}, and I_{tank} rotate with the same angular velocity of ω_{inj}, keeping ϕ and θ constant at ϕ_0 and θ_0, respectively [11].

As the frequency of injection signal (ω_{inj}) deviates farther from the self-resonance frequency of the ILO (ω_0), the phase shift introduced by Z_{tank} (ϕ_0) grows, as found in Fig. 2.1 (b), and the angle between I_{osc} and I_{tank}, which is depicted in Fig. 2.2 (c), becomes larger. If ω_{inj} keeps departing from ω_0 and finally reaches the edge of the lock range ω_L, the angle between the I_{osc} and I_{tank} reaches a maximum and will thus limit the lock range. For find

out the phase relation of each component, we have to derive equation about ϕ_0 and θ. Mathematical representation of the ϕ_0 can be derived using the law of *sin*, *cos* in Fig. 2.3 (a):

$$sin\,\phi_0 = \frac{B}{I_{tank}} \text{ and } sin\,\theta = \frac{B}{I_{inj}} \tag{2.4}$$

$$sin\,\phi_0 = \frac{I_{inj}}{I_{tank}} sin\,\theta = \frac{I_{inj}\,sin\,\theta}{\sqrt{I_{osc}^2+I_{inj}^2+2I_{osc}I_{inj}\,cos\,\theta}} = \sqrt{\frac{1-cos^2\theta}{\frac{I_{osc}^2}{I_{inj}^2}+1+2\frac{I_{osc}}{I_{inj}}cos\theta}} \tag{2.5}$$

For find out $\phi_{0,max}$, we can use differentiation.

$$\frac{dsin\phi_0}{dcos\theta} = \frac{1}{2}\cdot\left(\frac{\frac{I_{osc}^2}{I_{inj}^2}+1+2\cdot\frac{I_{osc}}{I_{inj}}cos\theta}{1-cos^2\theta}\right)^{\frac{1}{2}}\cdot\frac{\left(\frac{I_{osc}^2}{I_{inj}^2}+1+2\cdot\frac{I_{osc}}{I_{inj}}cos\theta\right)\cdot(-2co\quad)-(1-cos^2\theta)\cdot\left(2\cdot\frac{I_{osc}}{I_{inj}}\right)}{\left(\frac{I_{osc}^2}{I_{inj}^2}+1+2\cdot\frac{I_{osc}}{I_{inj}}cos\theta\right)^2} \tag{2.6}$$

To find the maximum, this derivative has to be zero. The first term in above equation does not vanish so possible solutions have to be found in the second term.

$$2I_{osc}I_{inj}cos^2\theta + 2\left(I_{osc}^2 + I_{inj}^2\right)cos\theta + 2I_{osc}I_{inj} = 0 \tag{2.7}$$

The two possible roots of this equation are

$$Soluition1:\ cos\theta = -\frac{I_{inj}}{I_{osc}} \tag{2.8}$$

$$Soluition2:\ cos\theta = -\frac{I_{osc}}{I_{inj}} \tag{2.9}$$

The second solution (2.9), however, results in $sin\phi_0 = 1$ which means the tank should provide a phase shift of 90°. An RLC tank can only provide this shift for $\omega\rightarrow\infty$ so the second solution (2.9) does not correspond to a real situation. The only solution (2.8) is thus

$$sin\,\phi_{0,max} = \frac{I_{inj}}{I_{osc}}\ \ for\ \ cos\theta = -\frac{I_{inj}}{I_{osc}} \tag{2.10}$$

The phase angle between I_{inj} and I_{osc} is $90° + \phi_{0,max}$. If I_{inj} decreases, I_{osc} must form a greater angle as to maintain the phase difference between I_{tank} and I_{osc}. Thus, minimum injection level for locking is

$$I_{inj} \geq I_{osc} \cdot sin\, \phi_{0,max} \tag{2.11}$$

To compute the value of corresponding to this case, we first note that the phase shift of the tank in the vicinity of resonance frequency. The transfer function of an RLC tank is given by

$$Z(j\omega) = \frac{j\omega L}{(1-\omega^2 LC)+\frac{j\omega L}{R}} \tag{2.12}$$

The phase characteristic thus equals

$$\angle Z(j\omega) = tan^{-1}\left(\frac{\omega L}{0}\right) - tan^{-1}\left[\frac{\omega L}{R\left(1-\frac{\omega^2}{\omega_0^2}\right)}\right] = \frac{\pi}{2} - tan^{-1}\left[\frac{\omega L}{R}\left(\frac{\omega_0^2}{\omega_0^2-\omega^2}\right)\right] \tag{2.13}$$

This expression can be re-written using the following property of inverse trigonometric functions

$$\frac{\pi}{2} - tan^{-1}x = tan^{-1}(x)^{-1} \tag{2.14}$$

The nominator of the argument can be approximated via

$$\begin{aligned} \omega_0^2 - \omega &= \omega_0^2 - [\omega_0 + (\omega - \omega_0)]^2 \\ &= -2(\omega - \omega_0)\omega_0 - (\omega - \omega_0)^2 \\ &\approx 2\omega_0(\omega_0 - \omega) \end{aligned} \tag{2.15}$$

The approximate expression for the tangent of the phase eventually becomes

$$tan\, \phi_0 = \frac{2Q}{\omega_0}\left(\omega_0 - \omega_{inj}\right) \tag{2.16}$$

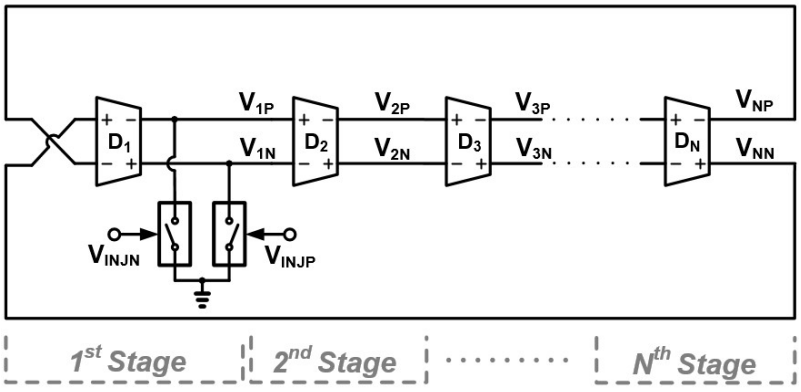
From Fig. 2.3 (b), $tan\, \phi_0 = \frac{I_{inj}}{I_{tank}}$, $I_{tank} = \sqrt{I_{osc}^2 - I_{inj}^2}$. The lock range is

$$\omega_L = (\omega_0 - \omega_{inj}) = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\frac{I_{inj}^2}{I_{osc}^2}}} \quad (2.17)$$

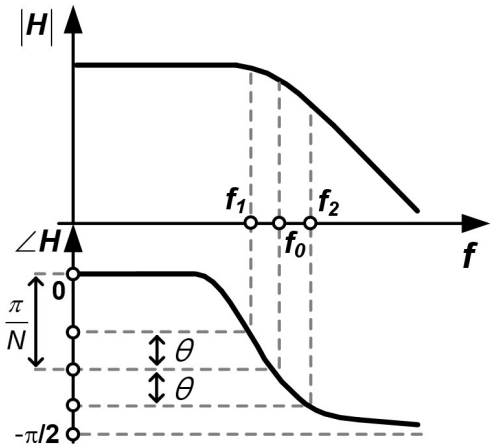
Where, Q means Quality factor of LC-tank. We denote this maximum difference by ω_L, with the understanding that the overall lock range is in fact $\pm\omega_L$ around ω_0. The lock range is proportional to the strength of injection current I_{inj} but inversely propotional to the Q-factor of LC tank. Hence, in the design of injection locked LC oscillator, to use High-Q LC tank decrease not only required current for free-runnnig, but also lock range. Note that ω_L is a function of Q, ω_0, $|Iosc|$, and $|Iinj|$. Since the values of Q, ω_0, and $|Iosc|$ are given by design, these values experience only a little change during operation, which is caused by the variations in the supply voltage and ambient temperature. In contrast, $|Iinj|$ can vary significantly and results in large variations of ω_L, as the amplitude of the received input signal changes. The lock range ω_L increases as the injection signal *Iinj* becomes stronger.

2.1.2 Injection Locked Ring Oscillator

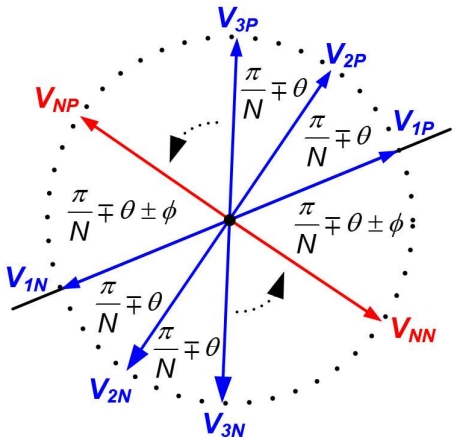
In this section, we discuss the detailed operation of the injection locked ring oscillator (ILRO), and in particular, the transient response of the injection locking process depending on whether the injection signal is higher or lower than the free-running frequency of the VCO. Primarily, the ILRO comprises a chain of interconnected delay cells as shown in Fig. 2.4 (a). Fig. 2.4 (a) shows a simplified linear model of the ring oscillator, which we have utilized for our mathematical analysis. The NMOS switch with the input V_{INJN} pulls down V_{1P} to GND when V_{INJN} is high. Given that V_{INJN} and V_{INJP} are complimentary to each other, V_{1N} remains floating as the V_{INJP} switch gets turned off. However, since V_{1P}



(a)



(b)



(c)

Figure 2.4 *N*-stage injection locked ring oscillator (a) frequency response of the delay cell (b) and a phase diagram for injection locking (c).

and V_{IN} are interconnected by a latch, V_{IN} is pulled high. The overall effect of the nodes V_{IP} and V_{IN} being pulled down and up is that the phase-delay contribution of the individual delay stages changes in response to the relative frequency of the injection signal to that of the free-running frequency, taking the ILRO to be locked to a frequency equivalent as that of the injection signal. To explain this, we consider the phase response of an individual delay stage when the ILRO is free-running and also when it is injection locked.

A delay cell in the *N*-stage ILRO can be modeled as a single pole amplifier, whose amplitude response rolls off at -20 dB/dec after the dominant pole and the phase difference

between the input and output reaches $-\pi/2$ radians at frequencies significantly higher the dominant pole as shown by the frequency response in Fig. 2.4 (b). In the ILRO, for the oscillation to sustain, the total phase shift of the loop must be a multiple of 2π so as to meet the Barkhausen criteria [12]. To meet this, an ILRO having even number of stages, has to cross couple the inputs to one of the stages from the previous stage's outputs. In this implementation 4th delay-cell inputs are cross coupled to 3rd delay-cell outputs. In the absence of an injection signal, each non-cross-coupled delay cells of the ILRO adds a phase of $(\pi+\pi/N)$, while the cross coupled delay cell adds a phase of π/N making sure that the Barkhausen criteria is met. Note, that this phase delay responses are valid only for ILROs with even number of stages. A given delay-cell introduces an intrinsic phase reversal equivalent to π radians to its input signal. In addition, a variable component equal to π/N that depends on the number of delay stages is also added. Note that the cross-coupled stage does not add the intrinsic phase reversal to its input. Since the intrinsic phase reversal of the delay remains constant irrespective of whether the injection signal is present, it can be omitted from the rest of the analysis and is not included in the frequency response shown in Fig. 2.4 (a). The effect of injection locking is that the variable phase-delay of each of the delay cells changes in response to the injection signal to move the ILRO frequency to a locked state. It can be shown that once the ILRO is locked to the injection frequencies of $f_0 \mp \Delta f$ (f_1 and f_2), the phase shift of the delay cell changes to $\pi/N \mp \theta$. The overall phase-shift can be expressed as:

$$\begin{cases} (N-1)\pi + N\left(\frac{\pi}{N} - \theta\right) + \phi = 2m\pi, & for \quad f_{INJ} < f_0 \\ (N-1)\pi + N\left(\frac{\pi}{N} + \theta\right) - \phi = 2m\pi, & for \quad f_{INJ} > f_0 \end{cases} \tag{2.18}$$

where, θ represents the amount of phase shift caused by the change in oscillation frequency as shown by the frequency response of the delay cell (Fig. 2.4 (a)), and ϕ represents the

additional amount of phase shift generated by first delay cell due to the signal injection. The factor *(N-1)π* is the sum of the intrinsic phase-shift introduced by all the delay cells in the ILRO and remains a constant. However, when injection locking occurs at a different frequency from the free-running frequency, for satisfying (2.18), the value of $\mp N\theta$ must be canceled by $\pm\phi$ so that the overall phase shift of the oscillator loop becomes $2m\pi$ (m=1, 2 …) to maintain oscillation at the input injection frequency. As shown in Fig. 2.4 (b), therefore, the phase shift of delay cell D_1, ζ', and the phase shift of other delay cells, ζ, when f_{INJ} is less than f_0, can be described as follows:

$$\begin{cases} \zeta = \frac{\pi}{N} - \theta, \\ \zeta' = \frac{\pi}{N} - \theta + \phi \ = \frac{\pi}{N} - \theta + N\theta \end{cases} \tag{2.19}$$

Similarly, the phase shift of delay cell D_1, ψ', and the phase shift of other delay cells, ψ, when f_{INJ} is greater than f_0, can be described as follows:

$$\begin{cases} \psi = \frac{\pi}{N} + \theta, \\ \psi' = \frac{\pi}{N} + \theta - \phi = \frac{\pi}{N} + \theta - N\theta \end{cases} \tag{2.20}$$

For find out value of θ, we consider the schematic of ILRO as shown in Fig. 2.4 (a). Let's assume that the model comprises equivalent output resistance (R) and load capacitance (C) for each delay cell stage. The linear model yields a first-order transfer function for each stage expressed as:

$$H(f) = \frac{-A}{1+j\frac{f}{f_0}} \tag{2.21}$$

Where, A is the gain of single stage delay cell, and f_0 can be calculated by

$$f_0 = \frac{1}{2\pi RC} \tag{2.22}$$

The ILRO can oscillate at f_{osc} since each stage should contribute π/N phase shift.

$$tan^{-1}\frac{f_{osc}}{f_0} = \frac{\pi}{N} \tag{2.23}$$

$$f_0 = \frac{1}{\tan\left(\frac{\pi}{N}\right)} \cdot f_{osc} \tag{2.24}$$

where, f_{osc} is the free-running frequency of the ring oscillator. Consequently, open-loop transfer function for each stage of ring oscillator is:

$$H(f) = \frac{-A}{1+j\tan\left(\frac{\pi}{N}\right)\left(\frac{f}{f_{osc}}\right)} \tag{2.25}$$

In the free-running state, f is equals to f_{osc} in equation. The phase shift of the one stage in the ring oscillator is π/N. But in injection locking state, f_{osc} moves to $f_{inj} = f_{osc} \pm \Delta f$. The phase shift of the one stage in the ring oscillator can be represented as:

$$\tan\left(\frac{\pi}{N} \pm \theta\right) = \tan\left(\frac{\pi}{N}\right)\left(\frac{f_{inj}}{f_{osc}}\right) \tag{2.26}$$

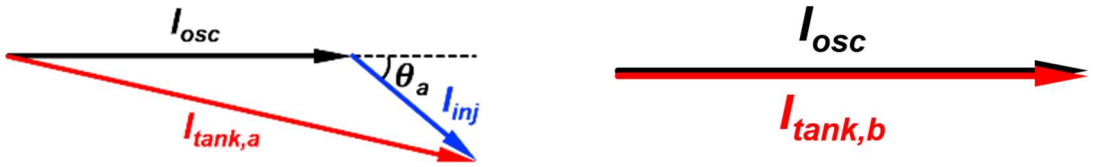
Hence, θ according to the oscillation frequency in the lock state can be expressed as [13]:

$$\theta = \left|tan^{-1}\left[tan\left(\frac{\pi}{N}\right)\frac{f_{INJ}}{f_0}\right] - \frac{\pi}{N}\right| \tag{2.27}$$

As a result, the phase shift of delay cell is changed from π/N according to the injection signal frequency.

2.2 Conversion Process of Injection Locked Oscillator

2.2.1 Conversion of OOK Signal



(a) **(b)**

Figure 2.5 Phasor diagrams of ILO currents for the OOK-modulated injection signal when: (a) I_{inj} is on and (b) I_{inj} is off.

Fig. 2.5 shows how the amplitude variations of the OOK-modulated input signal are preserved at the ILO output. When I_{inj} is on to present the data bit of '1', the I_{inj} is added to the I_{osc} to produce I_{tank}, and hence the amplitude of I_{tank} (= $|I_{tank,a}|$) becomes larger than that of I_{osc}:

$$\left|I_{tank,a}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos\theta_a} \tag{2.28}$$

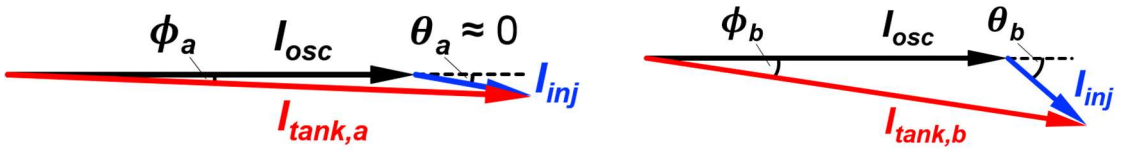
On the other hand, if I_{inj} is off to present the data bit of '0', the amplitude of I_{tank} (= $|I_{tank,b}|$) becomes the same as that of I_{osc}:

$$\left|I_{tank,b}\right| = |I_{osc}| \tag{2.29}$$

Multiplied by Z_{tank}, the I_{tank} generates the amplitude-modulated V_{out} signal.

In conclusion, the OOK input signal is also processed by the ILO to generate the amplitude-modulated signal at the output, as in the cases of BFSK and DBPSK input signal. Based on this conversion process of the ILO, an energy-efficient receiver IC can be constructed. The implementation details of the receiver circuits are described in the next section.

2.2.2 Conversion of BFSK Signal



(a) (b)

Figure 2.6 Phasor diagrams of injection locked LC oscillator currents for the FSK-modulated injection signal when: (a) $\omega_{inj} = \omega_a \approx \omega_0$ and (b) $\omega_{inj} = \omega_b = \omega_a + \Delta\omega$.

Assume that the injection frequency ω_a representing the data bit of '1' is set close to the self-resonance frequency ω_0 and hence $\theta_a \approx 0$ as depicted in Fig. 2.6 (a). Then, from (1), the $|I_{tank,a}|$ can be approximated as

$$\left|I_{tank,a}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos\theta_a} = |I_{osc}| + \left|I_{inj}\right| \tag{2.30}$$

The output voltage amplitude of the ILO corresponding to '1' (= $|V_{out,a}|$) is produced by the multiplication of $|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ ($\approx |Z_{tank}(\omega_0)|$). Since $|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ are close to the maximum possible values of $|I_{tank}|$ and $|Z_{tank}|$ respectively, $V_{out,a}$ presents nearly the largest output swing.

On the other hand, if the injection frequency $\omega_b = \omega_a + \Delta\omega$ used to indicate the data bit of '0' is set far from ω_0 but within the lock range, as shown in Fig. 2.6 (b), the $|I_{tank,b}|$ is given by

$$\left|I_{tank,b}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos\theta_b} \tag{2.31}$$

The output voltage amplitude of the ILO corresponding to '0' (= $|V_{out,b}|$) is derived by multiplying $|I_{tank,b}|$ with $|Z_{tank}(\omega_b)|$ ($< |Z_{tank}(\omega_0)|$). Since $|I_{tank,b}|$ and $|Z_{tank}(\omega_b)|$ are smaller than

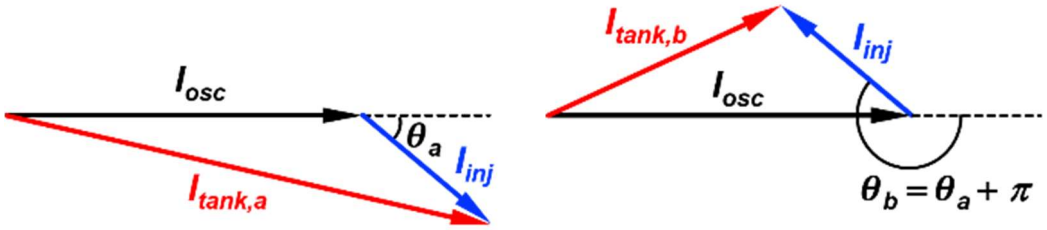
$|I_{tank,a}|$ and $|Z_{tank}(\omega_a)|$ respectively, $|V_{out,b}|$ is also smaller than $|V_{out,a}|$. How large amplitude difference between $V_{out,a}$ and $V_{out,b}$ is obtained for the frequency deviation of $\Delta\omega = |\omega_b - \omega_a|$ determines the frequency-to-amplitude conversion ratio.

Note that once the injection frequency ω_b for the data bit of '0' is determined, the corresponding phase shift ϕ_b is fixed as described in Fig. 2.1 (b). It can be found in Fig. 2.6 (b) that, for the same ϕ_b, if $|I_{inj}|$ increases, θ_b decreases, and hence cos θ_b approaches 1. In other words, the difference between $|I_{tank,a}|$ and $|I_{tank,b}|$ becomes smaller, and thus the frequency-to-amplitude conversion ratio decreases as $|I_{inj}|$ increases. It demonstrates the need for prohibiting any significant variations in the magnitude of I_{inj} to obtain a consistent demodulation performance over a wide range of received RF signal strength.

To achieve a good sensitivity, the receiver should be designed to operate even with a very weak RF input signal, which leads to a very small amplitude of I_{inj}. Since ω_L is narrow for small $|I_{inj}|$ as predicted by (7), the ω_a and ω_b cannot be separated too far from each other. The ILO-based receiver is therefore designed to generate a distinguishable amplitude change for such a small frequency difference when $|I_{inj}|$ is small. However, if a strong RF signal is received and hence the amplitude of I_{inj} increases, the ω_L becomes wide, and the frequency-to-amplitude conversion ratio reduces significantly, resulting in too small amplitude change at the ILO output to be discriminated properly. To avoid this problem, it is important to control the magnitude of I_{inj} to stay relatively constant.

2.2.3 Conversion of DPSK Signal

The conversion process from the DBPSK-modulated signal to the amplitude-modulated signal by the ILO is depicted in Fig. 2.7. Since I_{tank} is the vector sum of I_{osc} and I_{inj}, and V_{out}



(a) (b)

Figure 2.7 Phasor diagrams of injection locked LC oscillator currents for the PSK-modulated injection signal when: (a) (a) $\theta_{inj} = \theta_0$ and (b) $\theta_{inj} = \theta_0 + \pi$.

is the multiplication of I_{tank} and Z_{tank} when there is a phase change of π in I_{inj}, the amplitude of V_{out} changes accordingly [14].

When the ILO is in the injection-locked state, and I_{inj} forms the angle of θ_a with respect to the I_{osc} to represent the data bit of '1', $|I_{tank,a}|$ is given by

$$\left|I_{tank,a}\right| = \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos\theta_a} \tag{2.32}$$

as described in Fig. 2.7 (a).

If the angle between I_{inj} and I_{osc} changes to $\theta_b = \theta_a + \pi$ which corresponds to the data bit of '0', the ILO is perturbed from its injection-locked state and the magnitude of I_{tank} experiences an instantaneous change to $|I_{tank,b}|$, which is expressed as

$$\begin{aligned}\left|I_{tank,b}\right| &= \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos(\theta_a + \pi)} \\ &= \sqrt{|I_{osc}|^2 + \left|I_{inj}\right|^2 + 2|I_{osc}|\left|I_{inj}\right|\cos\theta_a}\end{aligned} \tag{2.33}$$

After this transient change, as the frequency of the injection signal does not change, the ILO returns to the injection-locked state, as shown in Fig. 2.7 (a) and the magnitude of I_{tank} settles back to $|I_{tank,a}|$. In other words, the output amplitude of ILO fluctuates when the phase of the injection signal changes abruptly.

As a result, the output amplitude of ILO fluctuates when the phase of the injection signal changes abruptly, and this amplitude variation can be captured by the following ED circuit, obviating the need for power-hungry circuit blocks such as the frequency synthesizer and mixer. Note that the output of the ED behaves like an RZ signal, which requires a conversion to the NRZ signal for input data recovery [14].

2.2.4 Frequency to Phase Conversion

To understand the concept of the injection locking process in the ILRO, we can consider the transient response of the output nodes of each of the ILRO delay cells. Several possible scenarios that show the relative alignment of an injection signal to the free-running VCO clock frequency (f_0) and how it modifies the phase-response of the ILRO clock outputs are shown Fig. 2.8. The illustration only shows the effect of a single injection signal pulse. As discussed earlier, in the absence of an injection signal, each of the delay cells introduce a variable phase-delay equivalent to π/N. We assume that the equivalent time-delay corresponding to a phase-delay of π/N is represented by Δt_{DEL}. The effect of the injection signals V_{INJP} or V_{INJN} are that it pulls down the nodes V_{1N} or V_{1P} to *GND* when one of them goes high. If either V_{1N} or V_{1P} are already at the *GND* level, the injection signal does not alter that node at all. Thus, the injection signal can affect the ILRO when both V_{1N} and V_{INJP} are high or when V_{1P} and V_{INJN} are high. The relative alignment of the injection signal and the free-running clock pulse can be summarized into four different scenarios:

- **Scenario 1:** The injection pulse V_{INJP} overlapping the rising edge of the free-run- ning clock V_{1N} as shown in Fig. 2.8 (a). The overlap interval between V_{INJP} and V_{1N} is denoted as Δt_{INJR}.

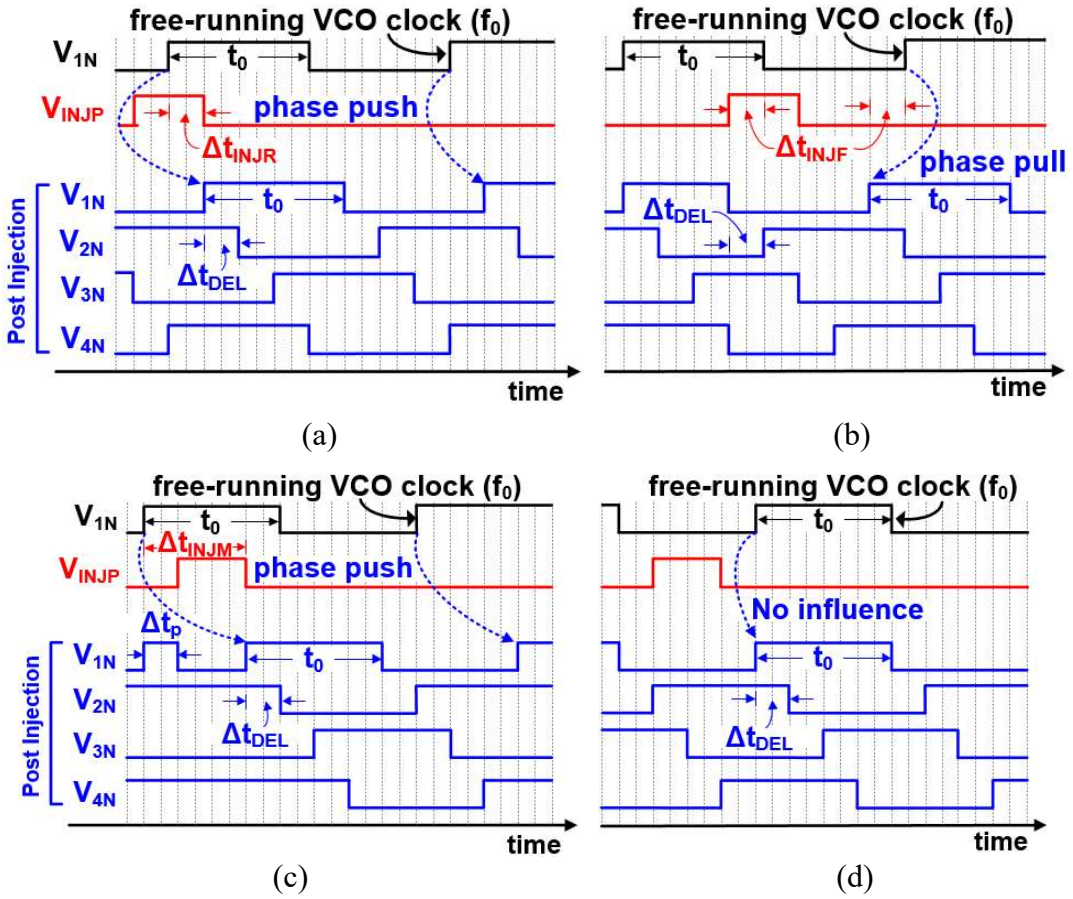


Figure 2.8 Change of 4-stage ILRO output according to injection position rising edge (a), falling edge (b), high state (c) and low state (d).

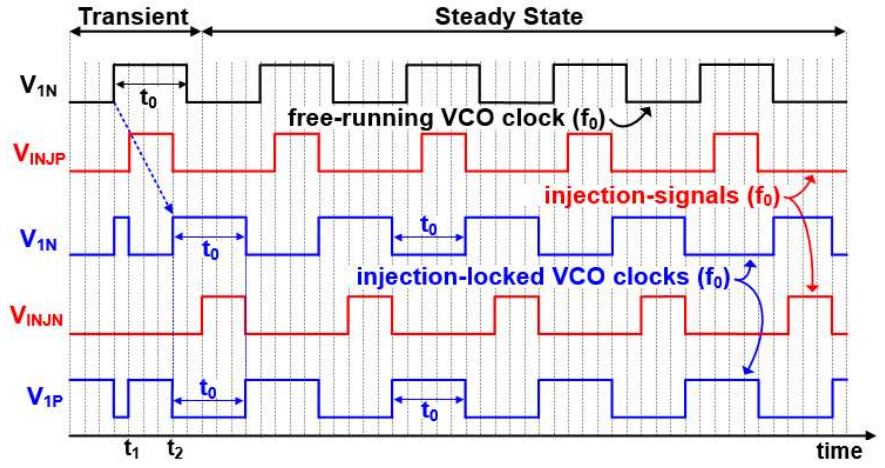
- **Scenario 2:** V_{INJP} overlapping the falling edge of the V_{IN} as shown in Fig. 2.8 (b). The overlap interval in this case is denoted as Δt_{INJF}.
- **Scenario 3:** V_{INJP} overlapping the high-state of V_{IN} as shown in Fig. 2.8 (c), where the time-interval between the rising edge of V_{IN} and the falling edge of the injection signal is Δt_{INJM}.
- **Scenario 4:** V_{INJP} overlapping the low-state of V_{IN} as shown in Fig. 2.8 (d).

When the injection signal V_{INJP} overlaps the rising edge of the free-running signal V_{IN}, (Fig. 2.8 (a)), the low state of the V_{IN}, is retained for an additional Δt_{INJR} time. The result of this is that the V_{IN} pulse is delayed by Δt_{INJR}. In contrast, when V_{INJP} overlaps the falling

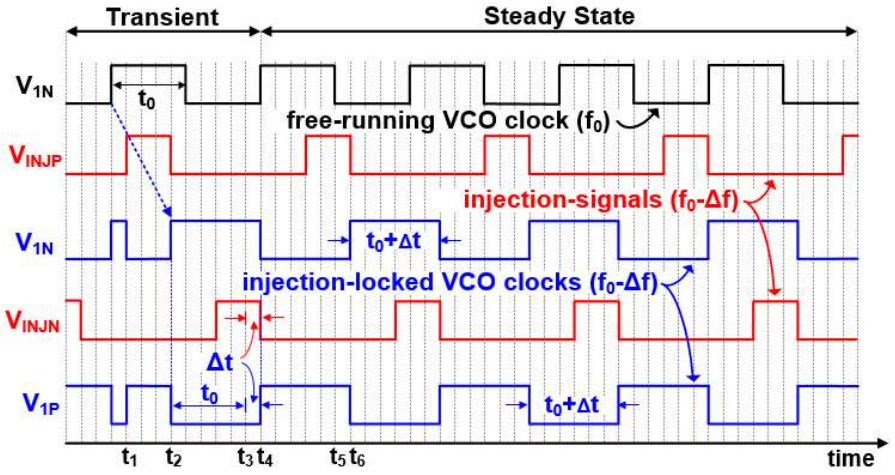
edge of V_{1N}, (Fig. 2.8 (b)), the injection signal pulls down V_{1N} earlier by Δt_{INJF}, causing the V_{1N} to advance by the same time-interval. When V_{INJP} overlaps with the high-state of V_{1N}, (Fig. 2.8 (c)), the effect on V_{1N} is similar to that of the case shown in Fig. 2.8 (a), where the rising edge is delayed. However, in this case, the delay time is equivalent to the time-interval between the rising edge of V_{1N} and the falling edge of the injection signal, Δt_{INJM}. Effectively, this scenario operation causes a glitch in the V_{1N} waveform, whose width is shown as Δt_p. If Δt_p is lower than the default delay time of the subsequent stages, it will not affect them as shown in Fig. 2.8 (c). However, if Δt_p is larger, this glitch would manifest in V_{2N}, V_{3N} and also V_{4N}. Irrespective of the magnitude of Δt_p, the fact that the rising edge would be delayed remains the same. Finally, the V_{INJP} has no effect on V_{1N} when it overlaps with its low-state as shown in Fig. 2.8 (d). In a practical operating scenario, a sequence of the above four cases lead the ILRO to be locked to a frequency equal to the injection signal.

To illustrate the locking mechanism further, the transition process from a free-running state to a locked state when the injection signal is applied to the middle of high state of free-running signal (shown in Fig. 2.8 (c)), is shown in Fig. 2.9. In practice, the relative alignment of the injection signal could possibly be any one of the scenarios mentioned in Fig. 2.8. However, this scenario is chosen for illustration as it involves the events shown in the other cases of Fig. 2.8 as will be discussed later.

The transient operation is discussed for cases when the injection signal frequency is equal to, lower and higher than the free-running frequency of the ILRO. Fig. 2.9 (a) shows the transient operation when the frequency of V_{INJP} is equal to the free-running frequency of the ILRO, V_{1N}. The V_{INJP} signal resets the node voltage V_{1N} to *GND* at the instant t_1. As the V_{INJP} goes low, the V_{1N} node rises to a high-state at t_2, thereby delaying the rising edge of



(a)



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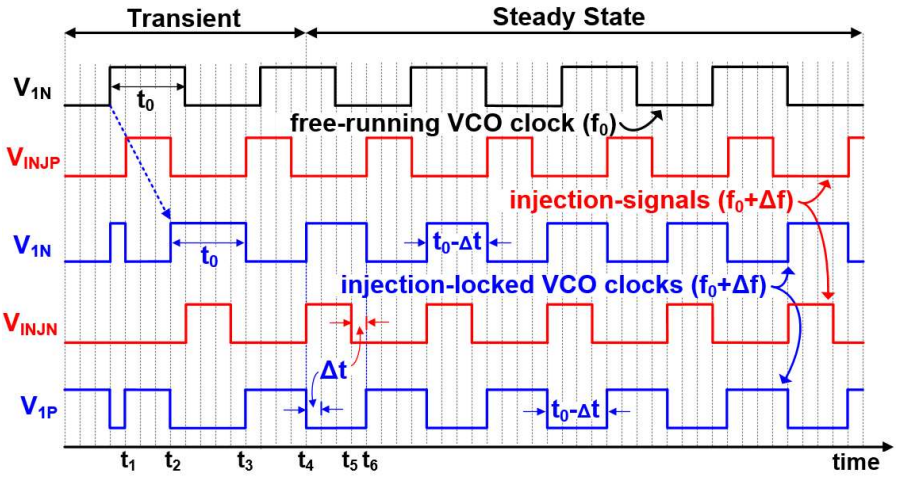
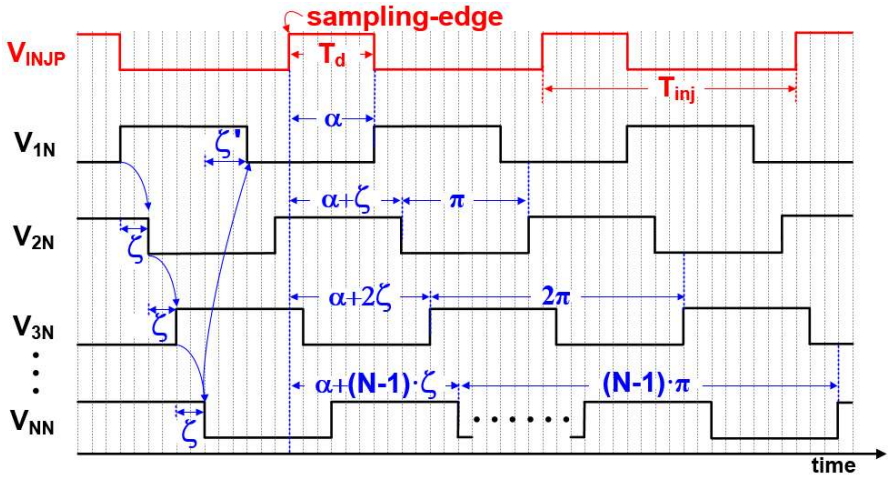


(c)

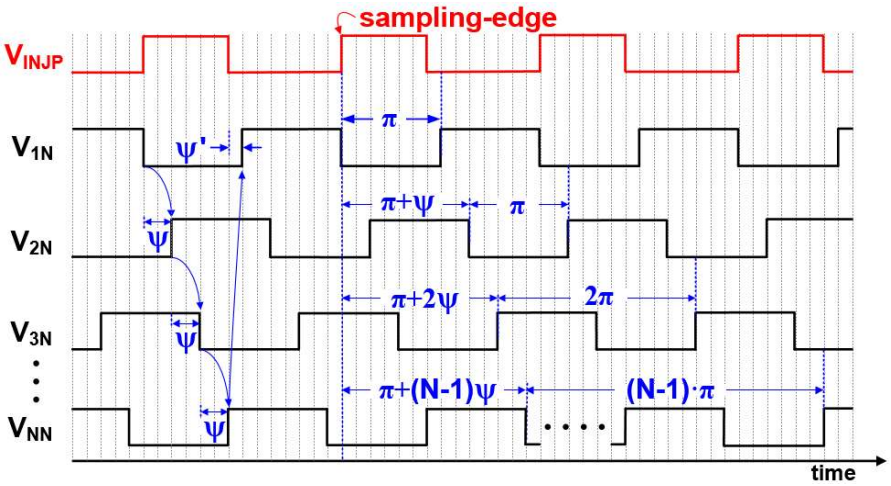
Figure 2.9 Injection-locking transient responses at $f_{INJ} = f_0$ (a), $f_{INJ} < f_0$ (b) and $f_{INJ} > f_0$ (c).

the free-running VCO clock. This is the scenario 3 of the locking process. Thereafter, the V_{INJP} or the V_{INJN} signals will not affect the ILRO operation, as they would overlap with the low-state of the V_{1N} and V_{1P}, which is the scenario 4 of the locking process. Thus, despite the phase-push introduced by V_{INJP} and V_{INJN}, the ILRO frequency remains the same. Fig. 2.9 (b) shows the transient operation when the frequency of V_{INJP} is lower than the free-running frequency the ILRO, V_{1N}. At the instant t_1, the V_{INJP} goes high, pulling down the V_{1N} to *GND*. At t_2, the V_{INJP} goes low, leaving V_{1N} floating. As a result, the rising edge of V_{1N} is delayed to the instant t_2, causing a phase-push (scenario 3). In the absence of the injection signal at V_{INJN}, the V_{1P} should have gone to a high-state at the instant t_3. However, as V_{1P} is pulled down by V_{INJN} until, t_4 the signal V_{1P} stays low for an extended period of Δt, thereby locking the ILRO to the lower injection frequency (scenario 1). Between t_5 and t_6, the V_{INJP} holds V_{1N} down to *GND* for an additional Δt (scenario 1). Once a lock is achieved, the scenario 1 repeats alternatively in V_{1N} and V_{1P}. When the injection signal frequency is higher than the free running frequency of the ILRO (Fig. 2.9 (c)), a phase-push happens and delays the rising edge of the V_{1N} to t_2 (scenario 3). Between t_2 and t_4, V_{INJN} and V_{INJP} go high without influencing the current state of V_{1P} and V_{1N} respectively as they are already at *GND* (scenario 4). However, at t_4, V_{INJN} pulls down V_{1P} to *GND*, causing the V_{1N} to rise to a high-state instantaneously (scenario 2). The overall effect of this is that the period is reduced by Δt, thereby locking the ILRO to the injection frequency that is higher than the free-running frequency. Once locked, the scenario 2 repeats alternatively in V_{1N} and V_{1P}.

In summary, the complimentary injection signals V_{INJP} and V_{INJN} introduces a phase-push/pull along with the widening or shortening of the ILRO outputs leading it to be locked with a frequency lower or higher than the nominal ILRO operating frequency.



(a)



(b)

Figure 2.10 Phase-relationships with the sampling edge at $f_{INJ} < f_0$ (a) and $f_{INJ} > f_0$ (b).

Fig. 2.10 shows the output waveform of each node of N-stage ILRO in the steady state after injection locking. When the ILRO is locked to an injection signal frequency that was originally lower its free-running frequency as shown Fig. 2.10 (a), the phase-delay between the successive edges between V_{NN} and V_{1N} becomes equal to $\zeta' = \pi/N - \theta + \phi$ as shown by equation (2.19). However, the delay between the successive edges of the other stages such as between V_{1N} and V_{2N}, V_{2N} and V_{3N} and so on remains at $\zeta = \pi/N - \theta$. The output is obtained by sampling one of the ILRO outputs using the injection locking clock. The fixed relative-

Table 2.1 Sapling State According to the Phase Difference

Output Stage	$f_{INJ} < f_0$ or $f_{INJ} > f_0$	
Even	$PD_k > k\pi$	Low
	$PD_k < k\pi$	High
Odd	$PD_k > k\pi$	High
	$PD_k < k\pi$	Low

phase relationship between the injection signal and the locked ILRO outputs enable latching one of the outputs at the sampling edge such that the output is registered as logic-high or logic-low. To explain this and to develop a closed form expression, the phase difference (PD) between the sampling edge of the input signal V_{INJP} and the successive rising edges of ILRO delay cell outputs V_{kN} can obtained as follows:

$$PD_k = \alpha + (k-1)\cdot\left(\pi + \frac{\pi}{N} - \theta\right) \quad for \quad f_{INJ} < f_0 \tag{2.34}$$

where *k* denotes the index of the stage from which the output is taken. In (2.34), α denotes a phase equivalent to a duty-cycle of $T_d \times 2\pi / T_{inj}$. Similar to this, a definite phase-relationship exists between V_{INJP} and V_{NN}, when the injection signal frequency is higher than the free-running ILRO frequency as shown in Fig. 2.10 (b). The phase-delay between the successive edges between V_{NN} and V_{1N} becomes equal to $\psi' = \pi/N + \theta - \phi$ from equation (2.20). However, the delay between the successive edges of the other stages such as between V_{1N} and V_{2N}, V_{2N} and V_{3N} and so on becomes at $\psi = \pi/N + \theta$. In this case, however, the PD between the sampling edge of the input signal V_{INJP} and the successive rising edges of ILRO delay cell of outputs V_{kN} can be shown as:

$$PD_k = \pi + (k-1)\cdot\left(\pi + \frac{\pi}{N} + \theta\right) \qquad for \quad f_{INJ} > f_0 \tag{2.35}$$

Using the relationships (2.34) and (2.35), an appropriate ILRO output can be sampled as the demodulator output as shown in Table 2.1. Due to the injection locking, a well-defined phase-relationship is established between V_{INJP} and the ILRO outputs V_{kN} and V_{kP}, where k refers to the state from which the outputs are taken. As shown in Table I, for an even stage, (k=2, 4…) if the total phase difference between the sampling edge and the rising edge of k^{th} delay cell output is greater than kπ, the output will be sampled as active low. On the contrary, if the phase difference is less than $k\pi$, the output will be sampled as active high. If the outputs are taken from the odd numbered stages (k=1, 3…) and the overall phase difference between the sampling edge and the rising edge of k^{th} delay cell output is higher than $k\pi$, the output will be sampled as active high. If the phase difference is lower than $k\pi$, the output will be sampled as active low.

Finally, as observed from (2.34) and (2.35), the sampled output state in the cases when f_{INJ} is greater or lower than f_0 depends on the duty-cycle of injection signal. As shown in Table I and using N=4 and k=2 (values used by this design as discussed later), the DFF samples the low-state when the duty-cycle is over 38 % and the high-state when the duty-cycle is less than 38 % when f_{INJ} is lower than f_0. However, when f_{INJ} is higher than f_0, the DFF is always sampled as a logic-low as shown by (2.35) and Table 2.1. Therefore, in this thesis, a duty-cycle of 25 % is used so as to provide a margin of 13 % from the maximum

2.3 Summary

The operation principle of the injection locked LC oscillator and ring oscillator investigated in this chapter. An injection locked LC oscillator can translates the signal modulated with various modulation schemes such as OOK, BFSK, and DBPSK into a simple amplitude-modulated signal in the lock range. Using these characteristics of injection locked oscillator, an energy-efficient injection locked LC oscillator based receiver supporting multi-mode can be implemented. Because, injection locked LC oscillator allows to use simple envelope detection circuit for frequency down-conversion and signal demodulation. The implementation details of the receiver circuits are described in the next chapter.

Furthermore, an injection locked ring oscillator can convert frequency to phase difference. Using this property, simple and ultra-low power FSK demodulator can be implemented. The details of the demodulator circuits are described in chapter IV.

III. Multi-Mode Receiver Based on an Injection Locked LC Oscillator

3.1 Overall Receiver Architecture

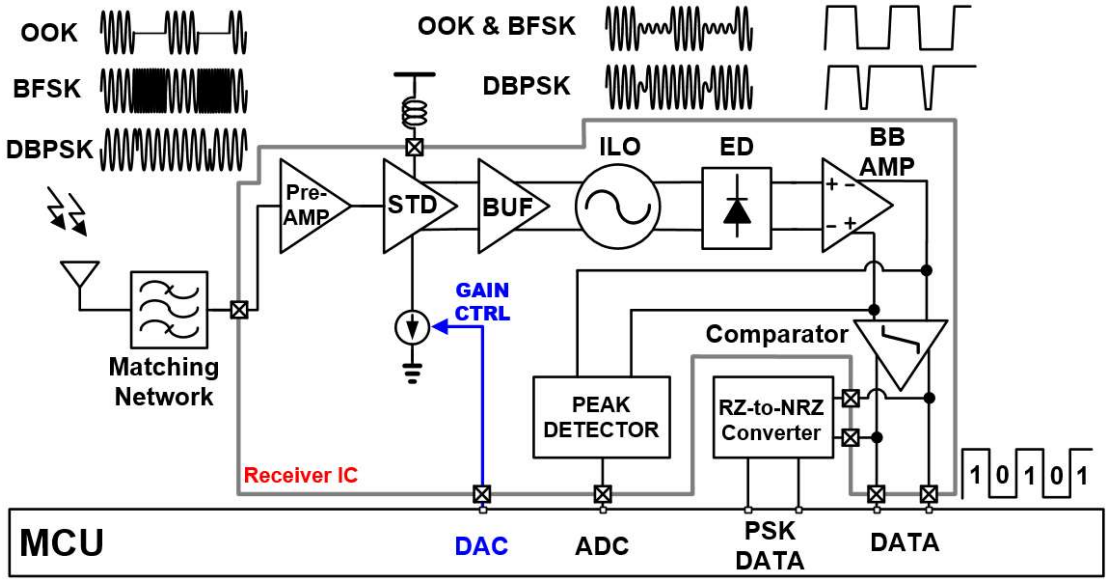


Figure 3.1 Overall architecture of the proposed wireless receiver system.

Fig. 3.1 is the block diagram showing the overall architecture of the proposed wireless receiver system, consisting of the front-end matching network, RF receiver IC, and micro-controller unit (MCU). In the RF receiver IC, the ILO converts the received OOK/BFSK/DBPSK signal to the amplitude-modulated signal. Based on such ILO operation, an energy-efficient wireless receiver can be realized by employing an envelope detector (ED) for RF-to-baseband frequency down-conversion and demodulation. The external MCU generates a gain control signal for the SDA based on the output amplitude of the baseband amplifier (BB AMP), which is measured by the peak detector. Through this closed-loop control, the magnitude of the RF signal injected to the ILO can be kept fairly

constant, and hence a significant change in the frequency-to-amplitude conversion ratio of the ILO can be prohibited when the BFSK signal is received.

The RF signal received by the antenna is fed to the preamplifier (Pre-AMP) through the matching network. The Pre-AMP amplifies the RF signal with moderate gain and provides isolation between the matching network and the SDA input to relieve the requirement of input-impedance matching for the SDA.

The SDA converts the single-ended input signal into an amplified differential signal driving the ILO. The *Q*-enhancement technique is applied to the SDA so that high gain can be achieved over a narrow frequency band. The high gain property allows obtaining the injection signal with an amplitude larger than the minimum required for locking the ILO even when the received RF signal is very weak, thereby enhancing the sensitivity of the receiver. Since the *Q*-enhanced SDA acts as a band-pass filter having a narrow passband, the selectivity of the receiver is also improved.

The differential output of the SDA is injected to the ILO, where the OOK/BFSK/DBPSK signal is converted into the amplitude-modulated signal. For the OOK signal, the ILO simply adds the constant amount of signal amplitude as explained in Section III, and thus the amplitude variations of the input signal are preserved at the ILO output. In the case of the BFSK signal, the ILO output has a large amplitude when the frequency of the injection signal (ω_{inj}) is close to the free-running frequency of the ILO (ω_0), while the output amplitude becomes small when ω_{inj} is far from ω_0. For the DBPSK signal, the output amplitude of ILO fluctuates when the phase of the injection signal changes abruptly. The ILO not only translates the OOK/BFSK/DBPSK signal to the amplitude-modulated signal but also improves the receiver sensitivity because the weak RF signal injected to the ILO generates the oscillator output signal having a relatively large swing.

The ILO output at RF is then converted down to the baseband by the ED. The baseband signal is further amplified by the BB AMP, and the BB AMP output is processed by the comparator to produce the final output data. Note that the output data for the DBPSK signal exhibits a return-to-zero (RZ) signal characteristic, as explained in Chapter II, from which the input data can be recovered by converting the RZ data to the non-return-to-zero (NRZ) data.

For reliable BFSK signal reception and demodulation, the frequency-to-amplitude conversion ratio of the ILO should not vary excessively. However, if the lock range of the ILO changes due to the varying magnitude of the injection signal, the frequency-to-amplitude conversion ratio doesn't stay constant, as explained in Section III. In this work, the strength of the ILO injection signal is regulated in a closed-loop manner, so that the ILO can provide a consistent frequency-to-amplitude conversion ratio. The peak detector in the receiver IC measures the amplitude of the BB AMP output, and this amplitude information is sent to the external MCU. Then, the digital-to-analog converter (DAC) embedded in the MCU generates the control signal to adjust the gain of the SDA, thus maintaining the strength of the ILO injection signal relatively constant.

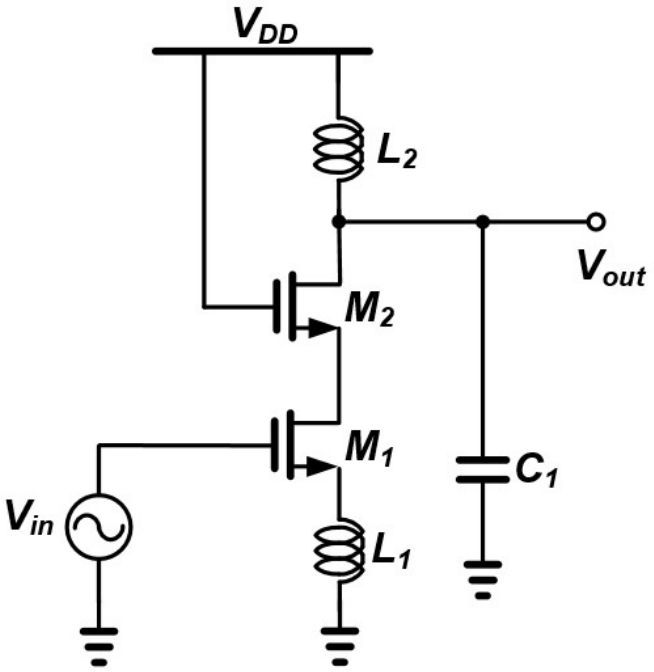
3.2 Details of the Blocks

We have examined the structure of the conventional receivers and the advantages and disadvantages of each structure in chapter I. In this chapter, circuits and operation principle of each block in the proposed receiver is described.

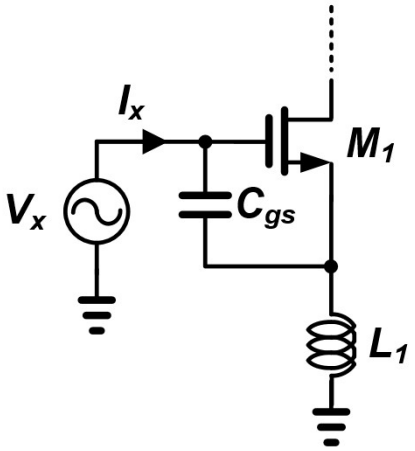
3.2.1 Pre-amplifier

A cascode pre-amplifier as shown in Fig. 3.2 (a) is typically used in ultra-low power receivers. The inductive load in Fig. 3.2 (a) can operate at lower supply voltages compared to structures with conventional resistive loads because the inductive load has a much lower DC voltage drop than the resistor. Furthermore, L_1 is able to operate at much higher frequencies than the resistive load by resonating with the total capacitance at the output node. Moreover, In the cascade structure, the change in the source of the cascode device M_2 is much smaller even though the output node voltage varies by ΔV[15]. This effect is called the shielding effect of the cascode element. The shielding characteristic of the cascade has an advantage of providing a stable matching characteristic by reducing the change of the input impedance according to the variation of the output impedance. Therefore, in the proposed receiver, the pre-amplifier used a cascode structure due to block the effect of the input impedance variation of SDA.

The schematic for calculating the input impedance of cascade amplifier is shown in Fig. 3.2 (b). Note that the gate-drain capacitance and source-bulk capacitance at the cascode common source is ignored. Since the gate-source voltage $I_x/C_{gs}s$ is formed through the



(a)



(b)

Figure 3.2 The pre-amplifier of the proposed wireless receiver (a) schematic (b) input impedance of cascode amplifier.

current I_x flowing through the C_{gs}, the drain current becomes $g_m I_x / C_{gs} s$. Since these two currents flow in L_1, the voltage is generated as follows.

$$V_p = \left(I_X + \frac{g_m I_x}{C_{gs} s} \right) L_1 s \tag{3.1}$$

Since $V_x = V_{gs} + V_p$, We have

$$\frac{V_X}{I_X} = \frac{1}{C_{gs1}s} + L_1 s + \frac{g_m L_1}{C_{gs1}} \tag{3.2}$$

Therefore, C_{gs} and L_1 can be selected so that third term which is frequency independent is 50 Ω. In fact, the inductor L_1 can be implemented with the inductance of wire bonding. Bonding wire must be inevitably used for connection of PAD to PCB. The effect of the bonding wire should also be considered in the circuit design. If the source pad is connected directly to the package or ground plane of the PCB using down bonding, it has a bonding inductance of about 0.5 to 1 nH.

The pre-amplifier of the receiver NF (Noise Figure) is added to the total NF of the receiver. Noise of the cascode element can be excluded from the NF calculation of the cascode structure [12]. Therefore, NF of the cascode structure can be calculated using Fig. 3.3. The noise of M_1 is represented by I_{n1}. The output current I_{out} can be calculated as follows:

$$I_{out} = g_m V_1 + I_{n1} \tag{3.3}$$

Since the voltage across L_1 equals to $L_1 s\left(I_{out} + V_1 C_{gs} s\right)$, applying *KVL* to the input loop

$$V_{in} = \left(R_s + L_g s\right) V_1 C_{gs} s + V_1 + L_1 s\left(I_{out} + V_1 C_{gs} s\right) \tag{3.4}$$

Substituting V_1 from (3.3)

$$V_{in} = I_{out} L_1 s + \frac{\left(L_1 + L_g\right) C_{gs} s^2 + 1 + R_s C_{gs} s}{g_m} \left(I_{out} - I_{n1}\right) \tag{3.5}$$

The input circuit resonates at frequency ω_0. $\left(L_1 + L_g\right) C_{gs} s^2 - 1 = 0$ at $s = j\omega$ since $\left(L_1 + L_g\right) C_{gs} = \omega_0^{-2}$. Therefore,

$$V_{in} = I_{out}\left(j L_1 \omega_0 + \frac{j R_s C_{gs} \omega_0}{g_m}\right) - I_{n1} \frac{j R_s C_{gs} \omega_0}{g_m} \tag{3.6}$$

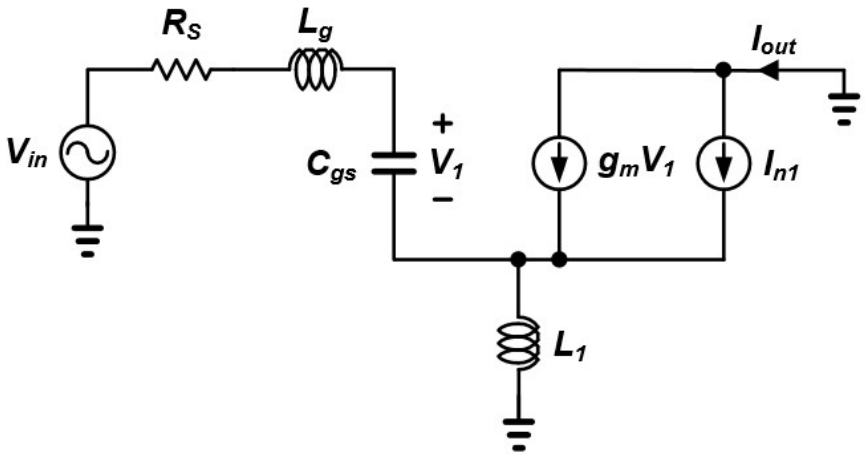


Fig. 3.3 Equivalent circuit of common-source stage for NF calculation.

The coefficient of I_{out} represents the trans-conductance gain of the circuit including R_S. In other words,

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{1}{\omega_0\left(L_1+\frac{R_SC_{gs}}{g_m}\right)} \tag{3.7}$$

Now, we need to satisfy $g_mL_1/C_{gs} = R_S$ in (3.2) for input matching. Since $g_m/C_{gs} = \omega_T$,

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{\omega_T}{2\omega_0}\cdot\frac{1}{R_S} \tag{3.8}$$

Under input matching conditions, the trans-conductance of the circuit is not related to L_1, L_g and g_m. If V_{in} is set to 0 in (3.6), the output noise by M_1 can be calculated by

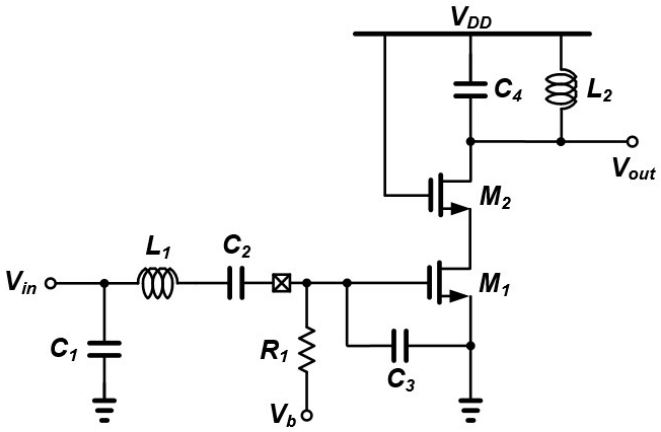
$$\left|I_{n,out}\right|_{M1} = |I_{n1}|\frac{R_SC_{gs}}{g_mL_1+R_SC_{gs}} \tag{3.9}$$

When, $g_mL_1/C_{GS} = R_S$,

$$\left|I_{n,out}\right|_{M1} = \frac{|I_{n1}|}{2} \tag{3.10}$$

Therefore,

$$\overline{\left|I^2_{n,out}\right|}_{M1} = kT\gamma g_m \tag{3.11}$$



M_1	20/0.18 um
M_2	10/0.18 um
C_1	1.39 pF
L_1	33 nH
C_2	100 pF
R_1	200 kΩ
C_3	100 fF
L_2	9.6 nH
C_4	190 fF

Figure 3.4. Proposed pre-amplifier.

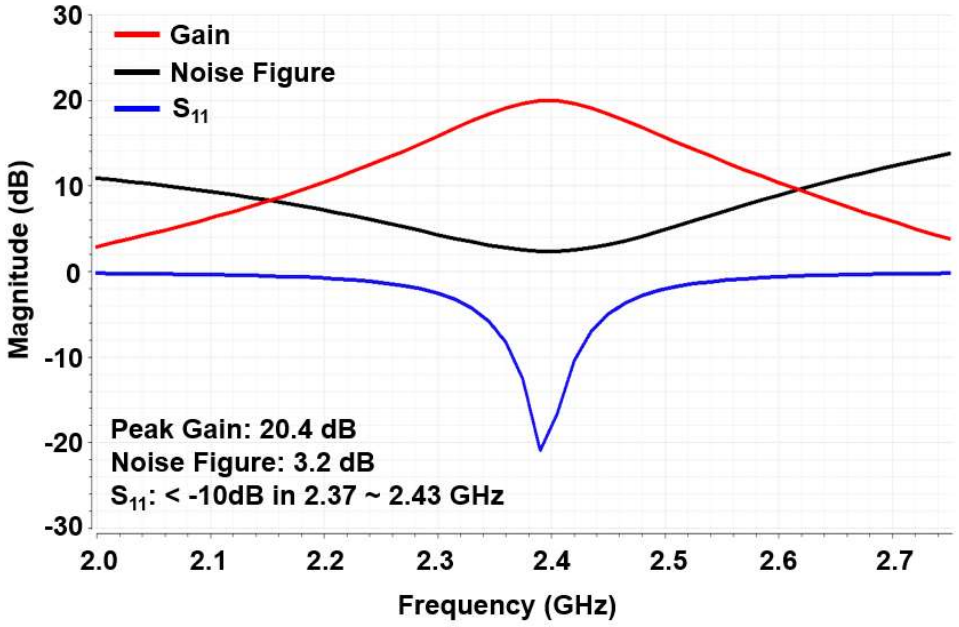


Figure 3.5 Simulation Result of pre-amplifier.

Divide the output noise by the circuit's trans-conductance and $4kTR_S$ and add 1 to the result, which is the noise figure of the cascade amplifier [3].

$$NF = 1 + g_m R_s \gamma \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{3.12}$$

This result is valid only when input matching is performed at the input resonance frequency. Now, the voltage gain of the cascode structure can be calculated. Assuming that

the output impedance of the cascode structure is much larger than R_1, the voltage gain of this structure can be expressed as the product of the trans-conductance of (3.8) and the load resistance R_1:

$$\frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0}\frac{R_1}{R_S} = \frac{R_1}{2L_1\omega_0} \tag{3.13}$$

Where R_1 represents the internal equivalent parallel resistance of the inductor. The design target of the pre-amplifier used in this study is shown in table 2. Based on the analysis of the cascode stage, the pre-amplifier is designed as shown in Fig 3.4 and each parameter of circuit are shown in table 3.

Fig. 3.5 shows the simulation results of the pre-amplifier. Impedance matching characteristics less than 10dB from 2.4 to 2.47 GHz. Also, Fig. 3.5 shows that the voltage gain is 26dB and the NF is 3.1dB. The power consumption is 57 uW.

3.2.2 Single to Differential Amplifier

Differential structure has the advantage of removing common mode noise efficiently than single-ended structure. Compared to single-ended injection, differential injection also greatly reduces the minimum amplitude for Injection locking in LC oscillator. Also, it is not enough to amplify the amplitude of signal for locking by one pre-amplifier. Therefore, a block that amplifies the input signal and converts it to a differential signal is required. The next stage of Pre-Amplifier is to place a STD to perform these functions. In this study, STD amplifier was designed using Q-enhancement technology and parallel oscillation circuit structure for high gain and signal conversion.

First, consider the equivalent circuit of a LC oscillator with negative resistance as shown in Fig. 3.6 to understand the operation of Q-enhancement. To find the voltage across the

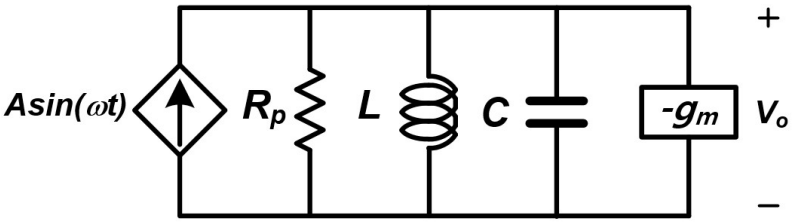


Figure. 3.6 Conceptual schematic of an LC oscillator with LC tank and negative conductance.

LC tank, we must first write the second order differential equation that describes the parallel RLC network given by

$$Asin(\omega t) = C\frac{dV_o}{dt} + \frac{1}{L}\int V_o d\tau + V_o G \tag{3.14}$$

Where, $G = R_p^{-1} + (-g_m)$, L is the tank inductance, C is the tank capacitance, and $Asin(\omega t)$ is the input excitation current. Assuming an underdamped system and solving for V_o, the resulting voltage across the LC tank is given by [16]

$$V_o = e^{-\alpha t}(A_1 cos(\omega_d t) + A_2 sin(\omega_d t)) + \frac{Asin(\omega t)}{\sqrt{G^2 + (\omega C - \frac{1}{\omega L})^2}} \tag{3.15}$$

Where,

$$\alpha = \frac{1}{2 \cdot \frac{1}{G} \cdot C} \tag{3.16}$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{3.17}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.18}$$

$$A_1 = V_0(0^+) \tag{3.19}$$

$$A_2 = \frac{\frac{d}{dt}V_0(0^+) + \alpha A_1}{\omega_d} \tag{3.20}$$

Where, $R_p = 1/G$. The term proportional to the exponential function in (3.15) describes the circuit's natural response while the term proportional to the input describes the response to an input signal. The oscillator operates in two different modes: $|-g_m| < R_p$

and $|-g_m| \geq R_p$. When $|-g_m|$ is larger than R_p, the oscillator is in amplifier mode and the amount of energy put into the circuit by the active devices is not enough to overcome the losses in the tank and oscillations will not build up. Under this amplifier mode condition, the natural response portion of the equation is negligible since previous oscillations were eliminated. This leaves the second term which describes the tank voltage resulting from the input signal.

When $|-g_m|$ becomes greater than R_p, resulting in α becoming negative. Now, the exponential term in (3.15) becomes dominant, and the circuit quickly builds oscillations. Under this condition, the response from the input becomes negligible compared with the exponential term. To simplify the analysis, the voltage on the tank is at its peak. Then

$$A_1 = \frac{A}{\sqrt{R^{-2}+(\omega C-1/\omega L)^2}} \tag{3.21}$$

$$A_2 = \frac{\alpha A_1}{\omega_d} \tag{3.22}$$

Above analysis gives two equations for the two different modes of operation in oscillator. First, when the oscillator is in amplifier mode, $V_{o,amp}$ is calculated as

$$V_{o,amp} = \frac{Asin(\omega t)}{\sqrt{R^{-2}+(\omega C-\frac{1}{\omega L})^2}} \tag{3.23}$$

and when the oscillator build up the free-running output, the output amplitude is represented as

$$V_{o,osc} = e^{-\alpha t}[A_1 cos(\omega_d t) + A_2 sin(\omega_d t)] \tag{3.24}$$

Where, A_1 and A_2 are given in (3.21) and (3.22), respectively. Another important parameter is the LC tank Q. The Q of the LC tank is described by [17]

$$Q = \omega_0 \frac{energy\ stored}{average\ power\ dissipated} = \frac{1}{\sqrt{LC}} \frac{\frac{1}{2}C(I_p R)^2}{\frac{1}{2}I_p^2 R} = \frac{|R|}{\sqrt{\frac{L}{C}}} \tag{3.25}$$

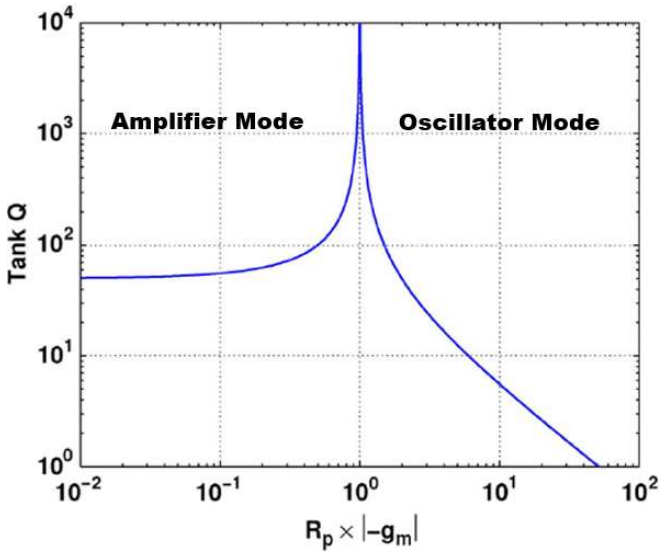
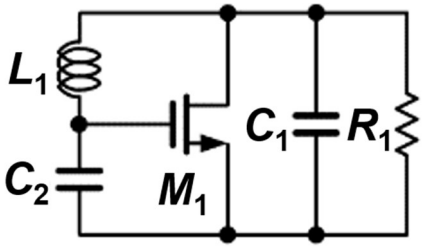
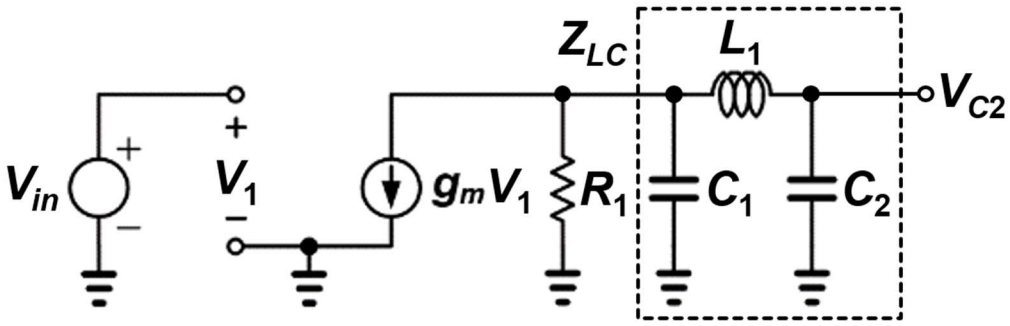


Figure 3.7 Tank Q for varying negative trans-conductance and a fixed R_p.

Where, R means sum of negative resistance $-1/g_m$ and R_p in the oscillator circuit. A high-Q factor results in a very narrow bandwidth in the LC Tank, which improves the receiver selectivity while also providing a higher voltage gain to the incoming signal when the oscillator is in amplifier mode. Fig. 3.7 illustrates the effect on tank Q from sweeping the $-g_m$ value in the circuit shown in Fig. 3.6. When the magnitude of $-g_m$ is very small compared with R_p, the resulting Q of the oscillator is determined by R_p. As the magnitude of $-g_m$ is increased, the Q also increases, approaching infinity, as the magnitude of $-g_m$ approaches $1/R_p$. Finally, as the magnitude of $-g_m$ continues to increase beyond R_p, the Q decreases approaching zero for very large values of $|-g_m|$. The regions to the left and right of 10^0 in Fig. 3.7 correspond to the amplifier mode and oscillation mode, respectively. Based on this characteristic, it is possible to implement a Q-enhanced amplifier with high gain and narrow bandwidth by operating the parallel resonant circuit as an amplifier and setting its $|-g_m|$value close to 1/*Rp* [18], [19].



(a)

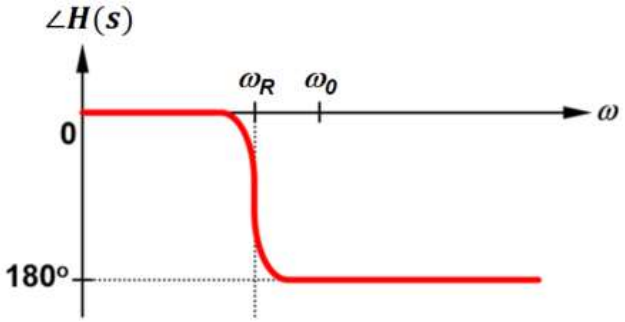


(b)

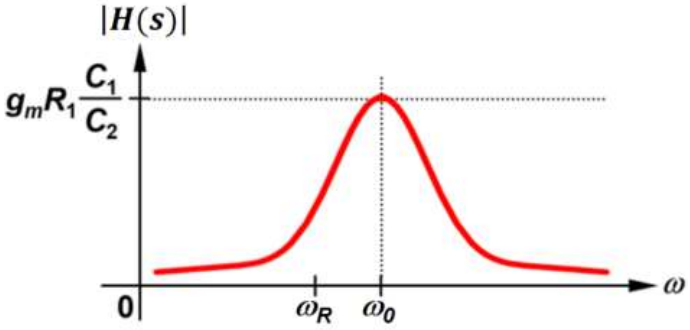
Figure 3.8 Oscillator structure (a)parallel oscillation circuit (b)small-signal equivalent circuit of parallel oscillator.

The core circuit of the proposed *Q*-enhanced SDA is based on the aforementioned parallel resonant circuit structure and its simplified schematic diagram is shown in Fig. 9(a). This circuit oscillates when the voltage at the drain node is 180^{o} out of phase with respect to the voltage at the gate node, and the negative conductance generated by the MOS transistor is larger than $1/R_1$. If we set the negative conductance value to be slightly smaller than $1/R_1$ and take the differential outputs from the gate and drain nodes, this circuit operates as a *Q*-enhanced SDA. The input signal is applied to the drain node in the form of current.

To investigate the operation of the circuit shown in Fig. 3.8 (a), the feedback loop of this circuit can be cut at the gate node of the MOS transistor to analyze the loop gain characteristic. By using the small-signal equivalent circuit given in Fig. 3.8 (b), the loop gain can be calculated as



(a)



(b)

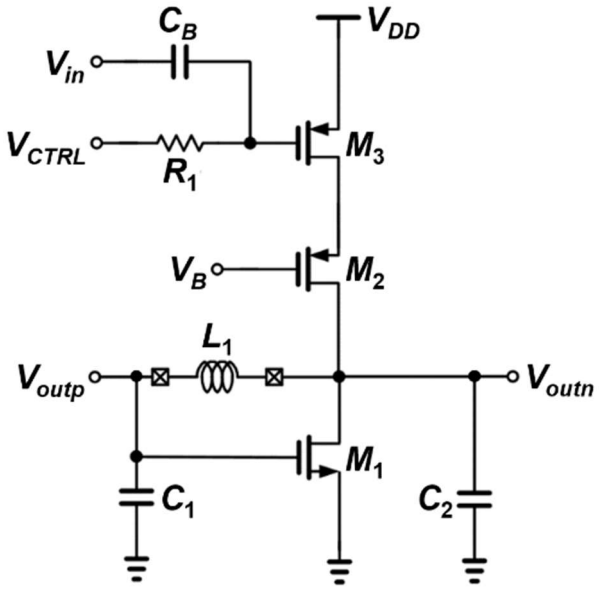
Figure 3.9 Transfer function (a)Phase vs. frequency characteristic of the voltage division factor and (b)magnitude vs. frequency characteristic of the loop gain and.

$$H(s) = \frac{V_{C2}}{V_{in}} = -g_m \frac{R \cdot Z_t}{R + Z_t} \cdot K \tag{3.26}$$

where Z_{LC} is the total equivalent impedance of the circuit network composed of L_1, C_1, and C_2, and K is the voltage division factor caused by the series-connected L_1 and C_2. K is expressed as

$$K = \frac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2} + j\omega L_1} = \frac{1}{1 - \frac{\omega^2}{\omega_R^2}} \tag{3.27}$$

Where, ω_R^2 means $1/L_1C_2$. Here, Note that K introduces a phase inversion at the frequencies higher than ω_R, as depicted in Fig. 3.9 (a). When it is lower than this frequency, phase inversion disappears. Z_t is given by



M_1	6 μm / 0.18 μm
M_2	4.5 μm / 0.18 μm
M_3	15 μm / 0.18 μm
L_1	6 nH
C_1, C_2	351 fF
R_1	320 kΩ
C_B	1.79 pF

Figure 3.10 Schematic diagram of the SDA.

$$Z_t = \frac{\frac{1}{j\omega C_1}\cdot\left(\frac{1}{j\omega C_2}+j\omega L_1\right)}{\frac{1}{j\omega C_1}+\left(\frac{1}{j\omega C_2}+j\omega L_1\right)} \tag{3.28}$$

Therefore, the voltage across capacitor C_2 is as follows.

$$\frac{V_{C2}}{V_{in}} = -g_m \frac{1}{j\omega(C_1+C_2)\cdot(1-\omega^2 L_1 C_1 \| C_2)+\frac{1}{R_1}(1-\omega^2 L_1 C_2)} \tag{3.29}$$

For the oscillation, the imaginary part of the denominator in (3.29) must be zero, if this circuit oscillates, the oscillation frequency is given by

$$\omega_0^2 = \frac{1}{L_1 C_1 \| C_2} \tag{3.30}$$

At the oscillation frequency, the magnitude of the loop gain is calculated as

$$\frac{V_{C2}}{V_{in}} = -g_m \frac{R}{1-\frac{1}{LC_1\|C_2}} = \left|g_m R_1 \cdot \frac{C_1}{C_2}\right| \tag{3.31}$$

which needs to be greater than 1 for the oscillation to occur. The magnitude of the loop gain shows the frequency characteristic, as presented in Fig. 3.9 (b). From (3.29) and (3.30), we can find that ω_0 is higher than ω_{inv}. Therefore, the feedback network causes a phase shift of 180° at ω_0, which is added to the phase inversion generated by the MOS

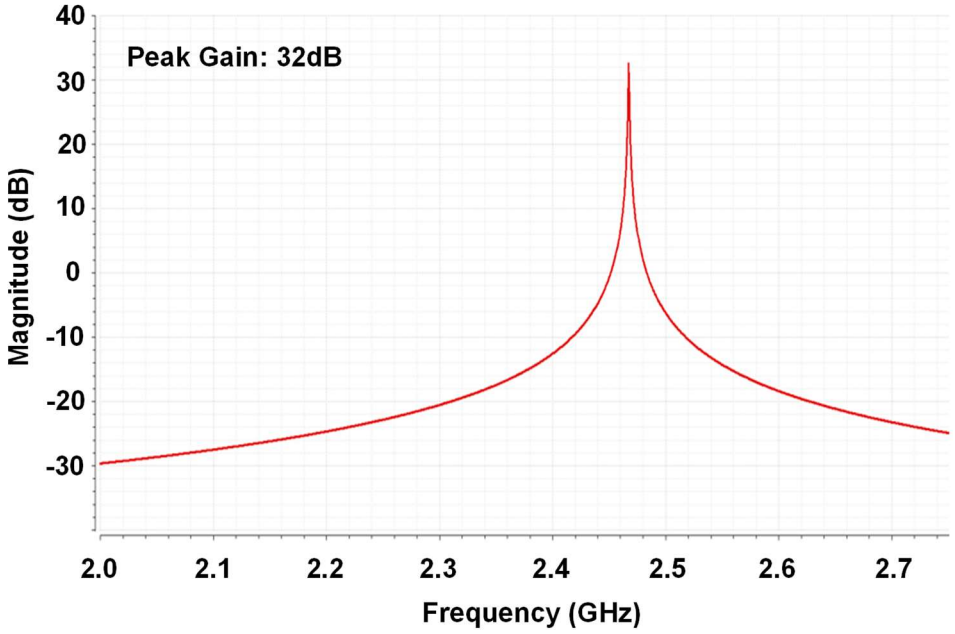


Figure 3.11 Gain of SDA.

transistor, leading to a total phase shift of 360º along the loop. If the transconductance value is controlled in such a way that the magnitude of the loop gain stays slightly lower than 1, the circuit can be operated as a *Q*-enhanced amplifier. Moreover, if the output voltages are taken from the gate and drain nodes of the MOS transistor while the input current is applied to the drain terminal, the circuit can also be used to convert the single-ended input to the differential output. The complete circuit diagram of the proposed *Q*-enhanced SDA is shown in Fig. 11. M_3 converts the input voltage V_{in} to the corresponding input current, which is fed to the drain node of M_1 through M_2. M_2 is used as a cascade element to provide isolation between the input and output terminals. The voltage gain of this *Q*-enhanced SDA can be controlled by adjusting the gate bias voltage V_{CTRL} of M_3. The V_{CTRL} determines the bias current flowing through M_1 and hence its transconductance, which in turn affects the *Q*–enhancement factor of the parallel resonant circuit formed by M_1, L_1, C_1, and C_2. If the inherent *Q* of the inductor L_1 is high, a large gain can be obtained with

flowing small bias current. In other words, by using a high-Q inductor, the power consumption of the Q-enhance SDA can be reduced. In this work, an off- chip inductor component having a high Q is used.

The center frequency and amplification gain of the SDA need to be tuned to accommodate the manufacturing process tolerances. We employ a tuning method similar to the one used in [15]. For frequency tuning, the V_{CTRL} is initially controlled to flow large enough bias current to oscillate the circuit. In the oscillation mode, the center frequency is tuned to the target value by controlling the capacitor banks C_1 and C_2. Once the frequency tuning is completed, the V_{CTRL} is adjusted again to enter the amplification mode and tune the amplification gain to the wanted value.

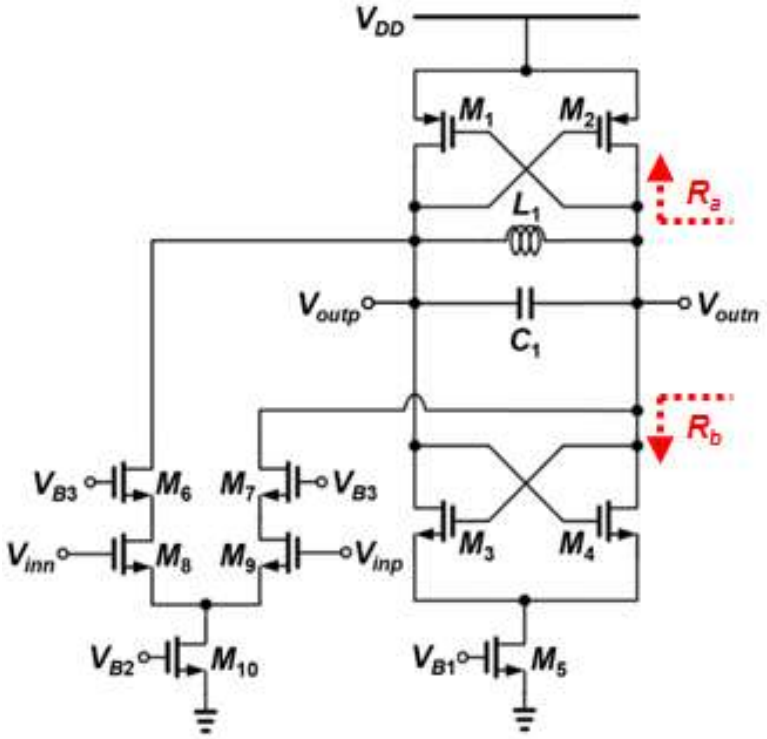
Fig. 3.11 shows the simulation result of combined gain of pre-amp and SDA. The voltage gain can be controlled by adjusting V_{CTRL} of STD. the 32 dB peak gain of SDA is obtained and the combined gain control range is 0 ~ 52dB. The power consumption of STD is 22uW. The high voltage gain and low power consumption are obtained by using the High-Q off-chip inductor.

3.2.3 Injection Locked LC oscillator

Fig. 12 presents the schematic diagram of the injection locked LC oscillator used in our design. In this paper, the complementary structure is applied to the injection locked LC oscillator. For oscillation, the total negative resistance must becomes

$$\frac{1}{R_a}+\frac{1}{R_b}+\frac{1}{R_f}\leq 0 \tag{3.32}$$

Where, R_f means equivalent resistance in Inductor. By using a cross-coupled pair that makes negative resistance on the top and bottom, negative resistance $R_a = -2/g_{mp}$ by



M_1, M_2	70 μm / 0.18 μm
M_3, M_4	50 μm / 0.18 μm
M_5	0.5 μm / 1 μm
M_6, M_7	1.5 μm / 0.18 μm
M_8, M_9	5 μm / 0.18 μm
M_{10}	2 μm / 1 μm
L_1	8.24 nH
C_1	40 fF

Figure 3.12 Schematic diagram of the ILO.

M_1 and M_2 and $R_b = -2/g_{mn}$ by M_3 and M_4 cancel the equivalent resistance of the inductor.

$$(g_{mn} + g_{mp})R_f \geq 1 \tag{3.33}$$

Hence, the proposed injection locked LC oscillator can be operated with low power consumption compare with typical differential structure.

The injection locked LC oscillator consists of a current injection circuit (M_{6-10}) and an oscillator core circuit (M_{1-5}, L_1, and C_1). In this topology, the complementary cross-connected MOS transistor pairs ($M_{1,2}$ for the PMOS pair and $M_{3,4}$ for the NMOS pair) provide negative resistance. The current injection circuit plays a role of converting the differential injection voltage to the differential injection current that is fed to the oscillator core circuit.

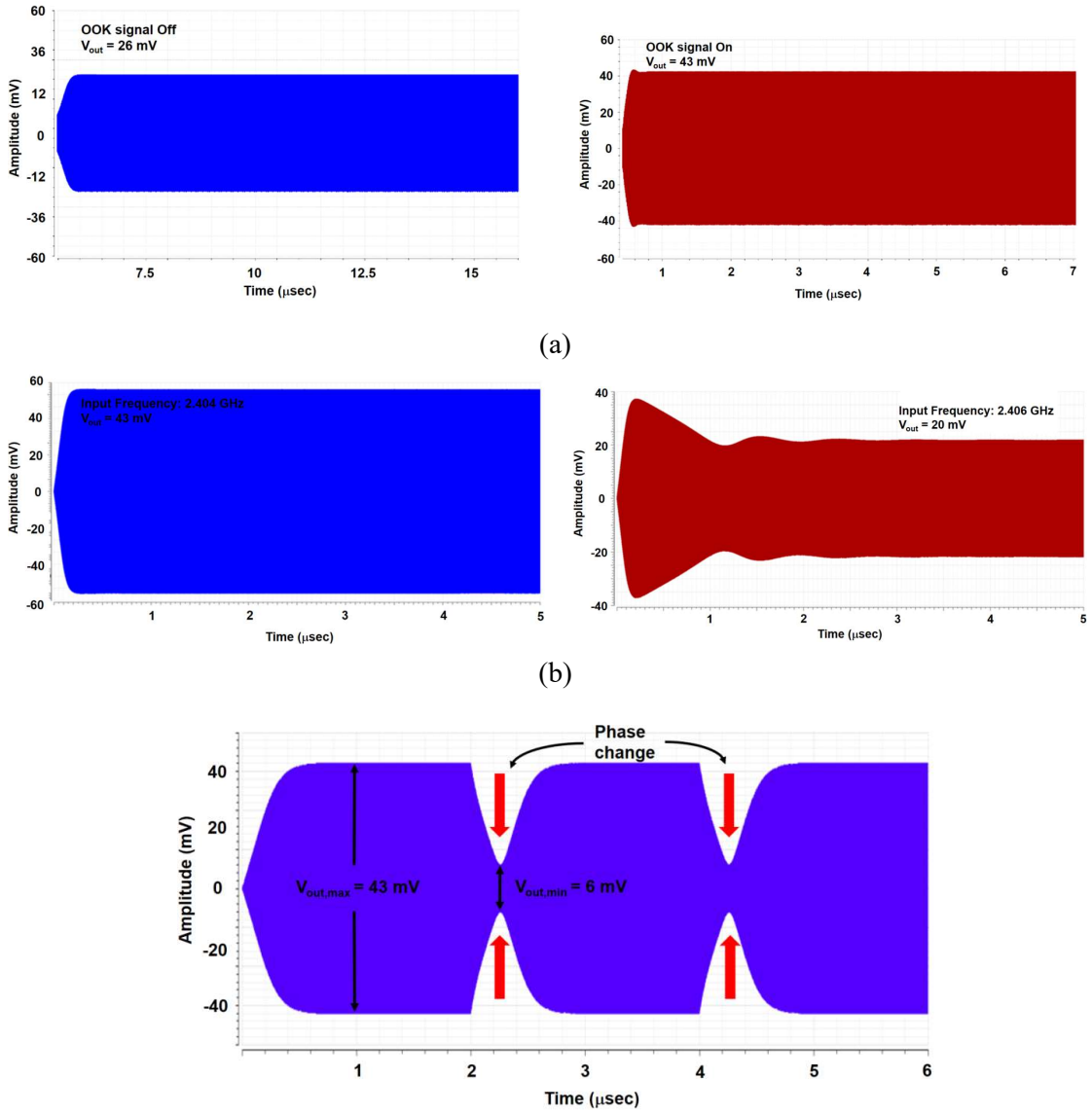


Figure 3.13 Simulation results: (a) OOK mode (b) BFSK mode (c) DPSK mode.

In the oscillator core, a capacitor bank is employed so that the free-running frequency of the injection locked LC oscillator can be tuned to the desired value.

Fig. 3.13 shows the injection locked LC oscillator simulation results. The free-running frequency of the injection locked LC oscillator is set to 2.404 GHz and the 2 MHz lock range is obtained when the amplitude of the input signal is 1.2mV. The power consumption of injection locked LC oscillator is 130uW. Fig. 3.13(b) presents the output waveform of the ILO when the OOK-modulated input signal is applied to the receiver. As explained in

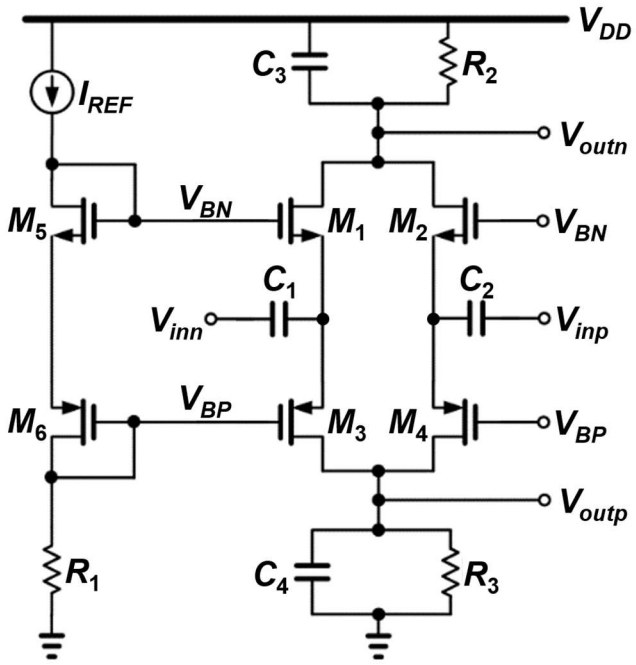
Section III-D, the amplitude variations of the OOK-modulated input signal are preserved at the ILO output, and thus the amplitude of the ILO output signal varies according to the input baseband data.

When the input frequency is equal to the free-running frequency, the peak amplitude of output voltage is 43mV as shown in Fig 3.13 (a) and when the input frequency is in the edge of the lock range (2.406 GHz), the output voltage is 20mV. As a result, it can be confirmed that frequency to amplitude conversion occurs.

In the case of DPSK as shown in Fig. 3.13 (c), digital data is expressed phase variation. The input signal undergoes 180˚ phase change, the ILO is perturbed from its injection-locked state, resulting in the instantaneous change of the ILO output amplitude. After the transient amplitude fluctuation, the ILO turns back to the injection-locked state, and its original output amplitude is recovered.

3.2.4 Fully Differential Envelope Detector

The schematic diagram of the fully differential ED is shown in Fig. 3.14 [20]. The non-linear *I-V* characteristics of the NMOS transistor $M_{3,4}$ and the PMOS transistors $M_{1,2}$ are used to down-convert the RF signal at the input to the baseband signal at the output. The common-gate topology is used, i.e., the input is applied to the source nodes of the transistors, and the output is taken from the drain nodes of the transistors. The low-pass filters, formed by $C_{3,4}$ and $R_{2,3}$ are placed to filter out high-frequency components produced by the nonlinear transfer function of the transistors. At the input nodes, the AC-coupling capacitors $C_{1,2}$ are employed to construct the high-pass filters when combined with the



M_1, M_2	10 μm / 0.18 μm
M_3, M_4	20 μm / 0.18 μm
M_5	10 μm / 0.18 μm
M_6	20 μm / 0.18 μm
C_1, C_2	1.79 pF
C_3, C_4	100 fF
R_1	120 kΩ
R_2, R_3	120 kΩ

Figure 3.14 Schematic of the proposed fully differential ED.

input resistances of the NMOS and PMOS transistors $M_{1,3}$ and $M_{2,4}$, respectively. The biasing circuit consists of stacked transistors $M_{5,6}$, I_{REF}, and R_1, where M_5 comprises the current mirrors with $M_{1,2}$ and M_6 constitutes the current mirrors with $M_{3,4}$. The core transistors M_1~M_4 are biased in the weak-inversion region. The amplitude of the differential output voltage is given by

$$I_d = I_Q e^{\frac{V_{in}}{nV_T}} \tag{3.34}$$

The 2nd order term of the power series expansion of (3.34) represents the small-signal baseband current

$$I_{d,N1} = I_Q \left[1 - \frac{V_{in}}{V_T} + \frac{V_{in}^2}{2V_T^2} - \cdots\right] \rightarrow i_{2nd} = \frac{I_Q V_{in}^2}{2V_T^2} \tag{3.35}$$

Applying a single-tone $V_{in}(t) = v_{id}(t)/2 = (A/2)sin(2\pi f_{in}t)$ at high frequency of $f_{in} = f_{RF} >> f_{LPF}$, the baseband output current i_0^- and the output voltage v_0^- at the output are given by

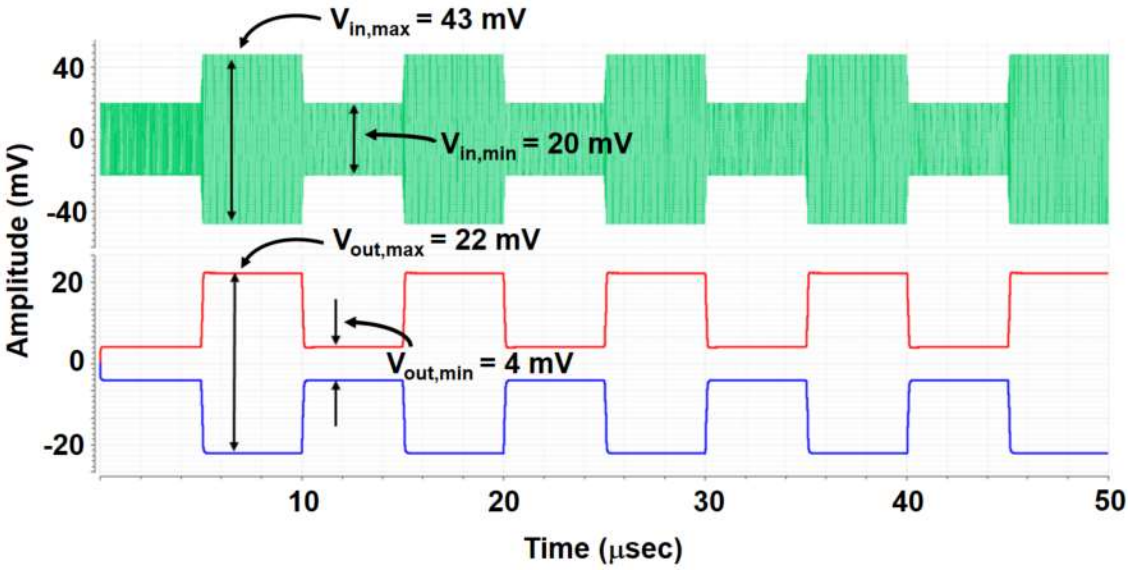


Figure 3.15 Transient simulation of envelope detector.

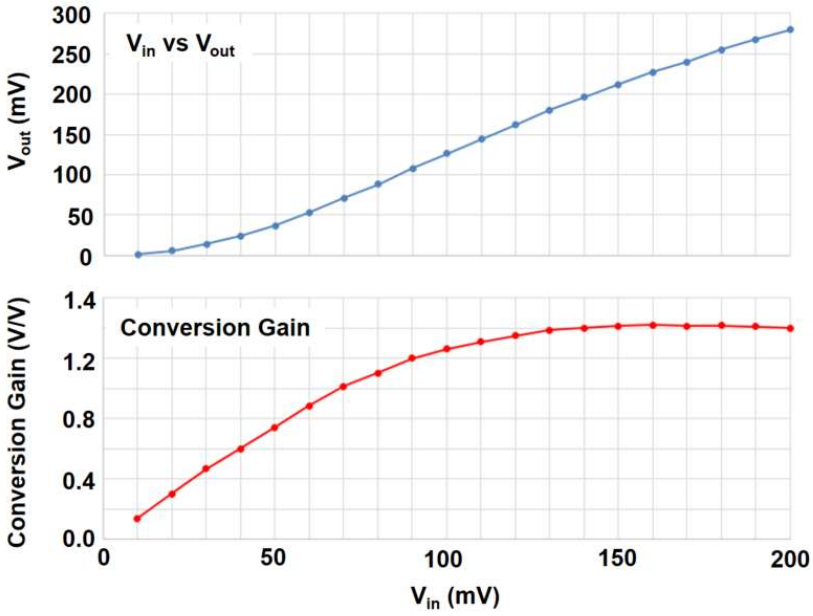


Figure 3.16 Conversion gain of envelope detector.

$$i_{2nd} = \frac{I_Q}{2V_T^2}\left[\frac{A^2}{8} - \frac{A^2 cos(4\pi f_{RF} \cdot t)}{8}\right] \rightarrow i_0^- = \frac{I_Q A^2}{16V_T^2} \rightarrow v_0^- = -\frac{I_Q R_L A^2}{8V_T^2} \tag{3.36}$$

The baseband output current i_o is negative, indicating that it flows from the output node to ground. As a result, a negative voltage drop occurs with respect to the bias point. A

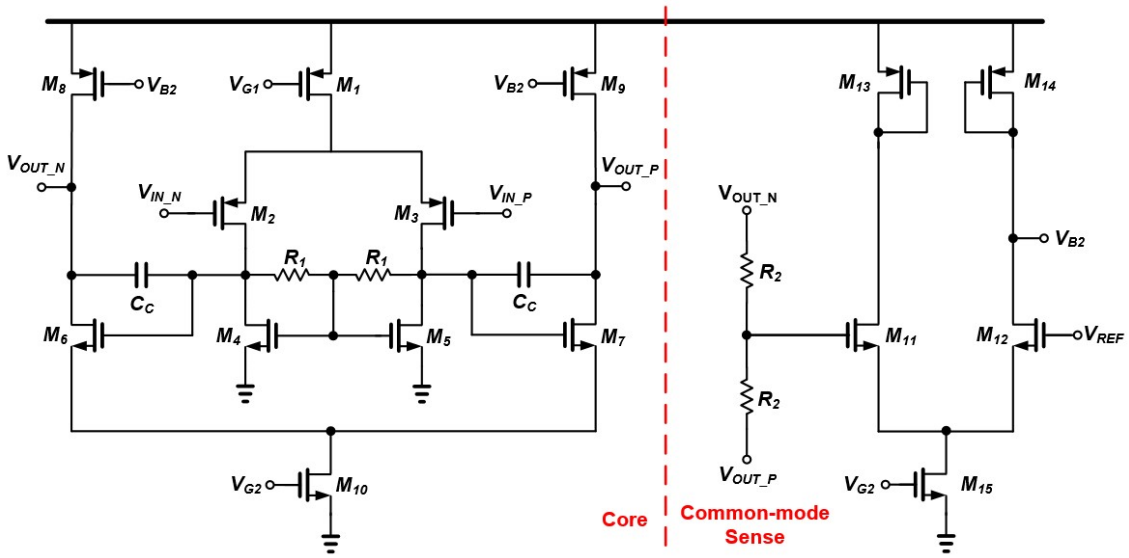
similar analysis can be done for the PMOS transistor. In this case, a positive voltage drop occurs with respect to the bias point. The resulting differential output voltage amplitude is then given by

$$v_{out} = V_{outp} - V_{outn} = \frac{I_Q R_L A^2}{4V_T^2} \tag{3.37}$$

The transient simulation results of the envelope detector are shown in Fig. 3.15. The output amplitude of the injection locked LC oscillator was assumed to vary from 47 mV to 20 mV. When the input amplitude varies 47mV to 20mV, the output of the envelope detector was 36 mV and 4 mV, respectively. Fig. 3.16 shows the conversion gain of the envelope detector. As the input size increases, the conversion gain increases. When the input signal exceeds a certain limit, the output is saturated due to the nonlinear characteristic.

3.2.5 Base-band Amplifier

The fully differential op amps, which have a differential input and produce a differential output. Fully differential op amps are widely used in modern integrated circuits because they have some advantages over their single-ended counterparts. They provide a larger output voltage swing and are less susceptible to common-mode noise. In addition, even-order nonlinearities are not present in the differential output of a balanced circuit. A balanced circuit is symmetric with perfectly matched elements on either side of an axis of symmetry. A disadvantage of fully differential op amps is that they require two matched feedback networks and a common-mode feedback circuit to control the common-mode output voltage.



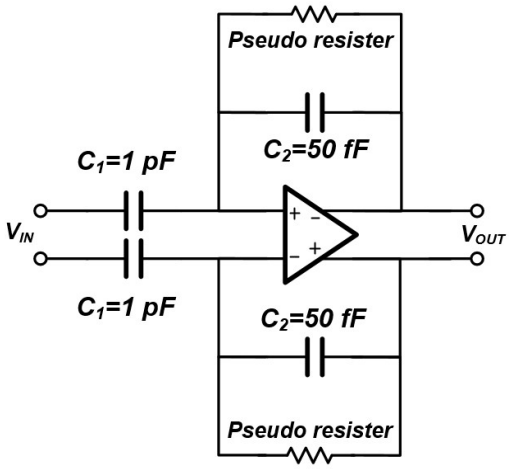
$M_{2\text{-}3}$,	20 μm / 1 μm	$M_{10,15}$	10 μm / 15 μm
$M_{4\text{-}5}$	2 μm / 15 μm	$M_{11\text{-}12}$	24 μm / 2 μm
$M_{6\text{-}7}$,	24 μm / 2 μm	$M_{13\text{-}14}$	14 μm / 5 μm
$M_{8\text{-}9}$	14 μm / 5 μm	C_c	50 fF
M_1,	20 μm / 5 μm	R_1, R_2	Pseudo Resistor

Figure 3.17 Schematic of fully differential amplifier

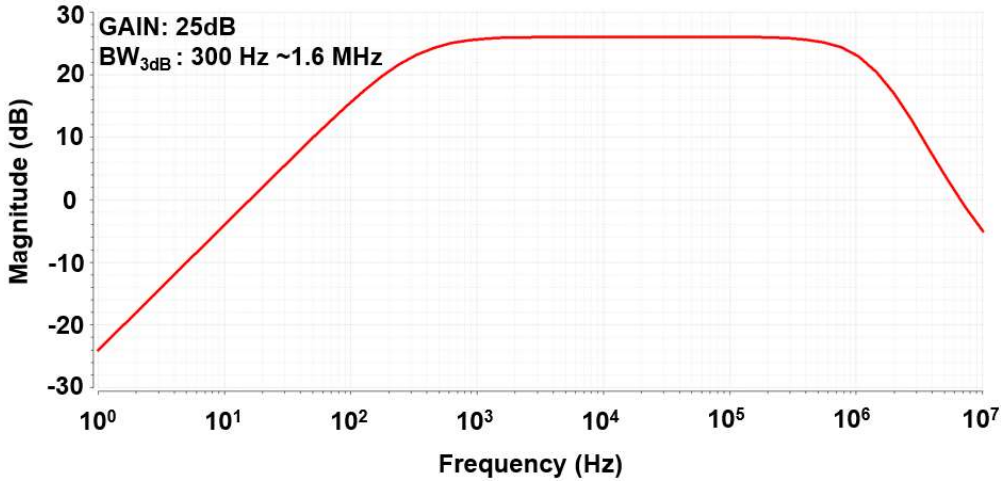
The 2-stage fully differential amplifier used in this paper is shown in Fig 3.17. The first stage consists of a common-source stage with a diode connection load, and the second stage consists of a common-source stage with a PMOS load. This amplifier, consisting of $M_{11} \sim M_{14}$, has diode connection load and is used for common-mode feedback. C_c is a device for the pole frequency compensation method using the Miller effect. The open loop gain of the amplifier can be calculated by

$$A_v = g_{m2,3}\left(r_{o2,3} \| r_{o4,5} \| R_1\right) \cdot g_{m6,7}\left(r_{o6,7} \| r_{o8,9}\right) \tag{3.38}$$

The circuit diagram for the simulation of OTA is shown in Fig. 3.18 (a). In this circuit, the voltage gain is determined by the ratio of C_1 and C_2 [15]. The simulation results are shown in Fig.3.18 (b). The voltage gain of 25dB is obtained and operating bandwidth is from 300Hz to 1.6 MHz.



(a)



(b)

Figure 3.18 BB AMP (a)schematic for simulation (b) simulation result.

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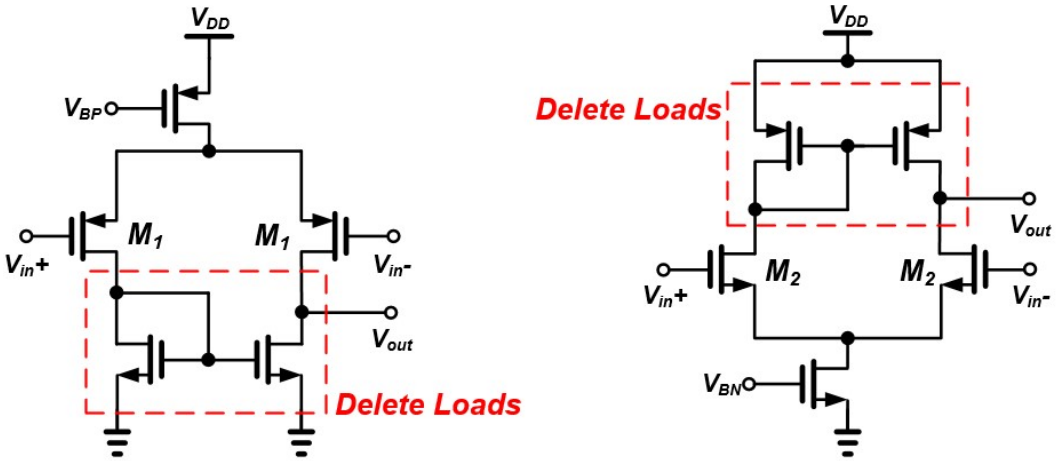
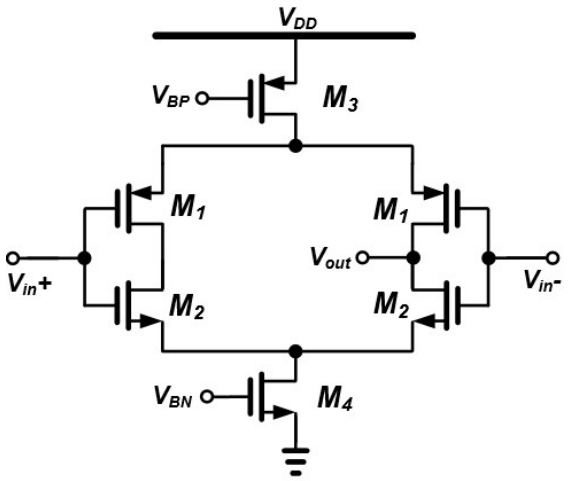
3.2.6 Fully Differential Comparator

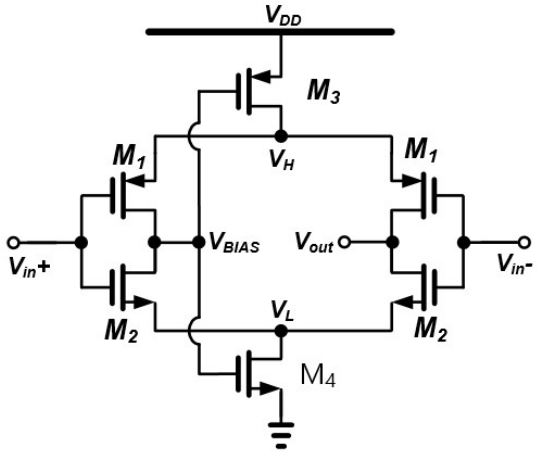
The basic operation of the complementary self-biased differential amplifier (CSDA) is perhaps most readily understood by following its derivation from well-known conventional CMOS amplifier configurations [21]. Fig. 3.19 (a) illustrates two conventional CMOS differential amplifiers, each the complement of the other. In the first step of the



(a)

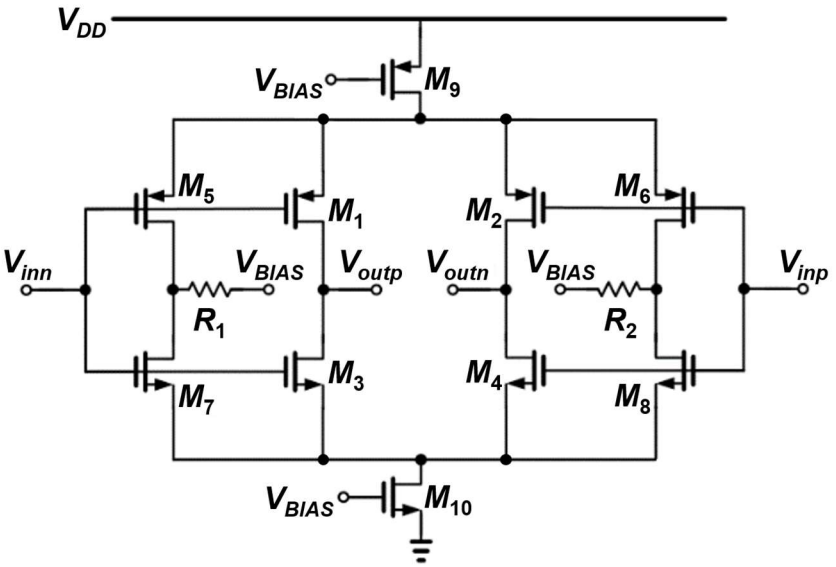


(b)



(c)

Figure 3.19. Derivation of complementary self-bias amplifier (a) conventional amplifier (b) external bias amplifier (c) complementary self-bias amplifier.



M_1, M_2, M_5, M_6	4 μm / 1 μm	M_3, M_4, M_7, M_8	2 μm / 1 μm	M_9	20 μm / 1 μm
M_{10}	5 μm / 1 μm	R_1, R_2	Pseudo - resistor	-	-

Figure 3.20 Schematic diagram of the fully differential comparator.

derivation, the loads from both amplifiers are deleted, and the input-pair drains of one amplifier are connected to the input-pair drains of the other. The resulting fully complementary, but externally biased, configuration is illustrated in Fig. 3.19 (b). However, this circuit cannot be biased in a stable fashion. In order for the circuit to be biased in a stable fashion, the currents through devices M_1, and M_2, must be identical. Any difference in currents through these two devices would result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig. 3.19 (b) is impractical. A simple modification to the circuit of Fig. 3.19 (b), however, results in a complete stabilization of the bias voltages. This modification is illustrated in Fig. 3.19 (c), in which the two bias-voltage inputs are disconnected from the external sources and are instead connected to the internal

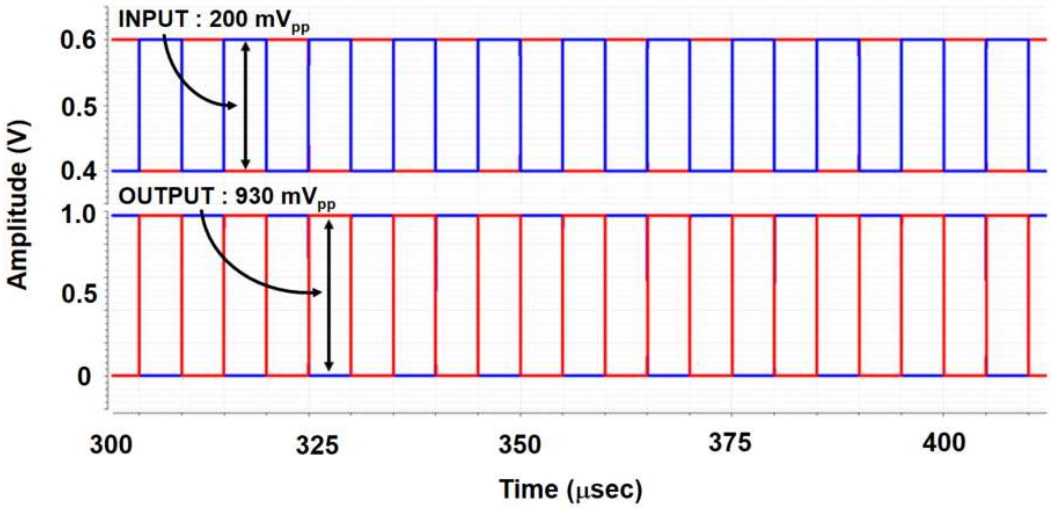


Figure 3.21 Simulation result of fully differential comparator.

amplifier node V_{BIAS}. This self-biasing of the amplifier creates a negative-feedback loop that stabilizes the bias voltages. Any variations in processing parameters or operating conditions that shift the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. In the CSDA, devices M_3, and M_4 operate in the linear region. Consequently, the voltages V_H and V_L, may be set very close to the supply voltages. Since these two voltages determine the output swing of the amplifier, the output swing can be very close to the difference between the two supply rails.

Using this characteristic, CSDA can be applied to the fully differential comparator as shown in Fig. 3.20. R_1 is used to extract the common mode voltage, which is used as the voltage to control the current sources M_3 and M_4, and the common mode voltage becomes the reference voltage of the comparator. Fig. 3.21 shows the simulation result of fully differential comparator. It can be seen that even when the input signal amplitude is 100mV, the function of the comparator is performed around the reference voltage of 500 mV. In addition, the amplitude of the output voltage swings from V_{SS} to V_{DD}.

3.2.7 Peak Detector

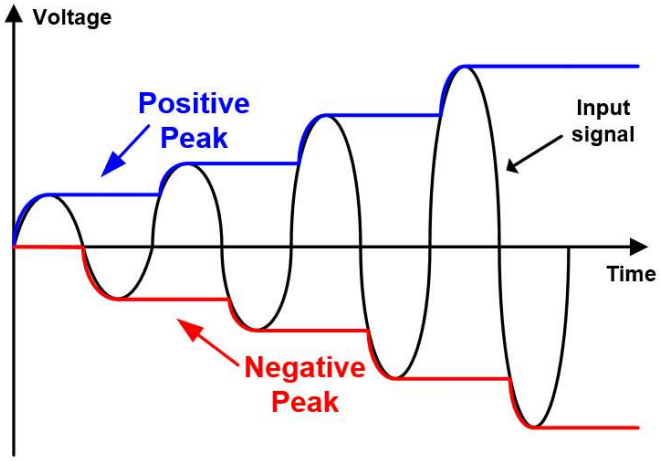


Figure 3.22 Ideal peak detector outputs.

Peak detectors are commonly found in modern communication receivers mainly as a building block of automatic gain control (AGC) loops. The main function of the peak detectors is to detect the peak value of an input signal. A positive peak detector is to follow the maximum value of an input signal and a negative peak detector is to trace the minimum value of the input signal. Fig. 3.22 illustrates ideal peak detector outputs from both peak detectors.

The peak detectors have two major problems: droop and slew rate. The droop is a slow discharge from the hold capacitor through the leakage and the path provided by the following stage, and it makes the output peak voltage deviate from the true peak value. It is better to reduce the droop for accuracy.

The slew rate is about the speed of charging the hold capacitor. It is better to increase the slew rate for speed. To increase the speed of the peak detector for tracing a fast input waveform, the value of the hold capacitor should be reduced. However, the smaller capacitor will cause the larger droop because it can discharge quickly. Therefore, there is a trade-off between low droop rate and high slew rate in peak detector design.

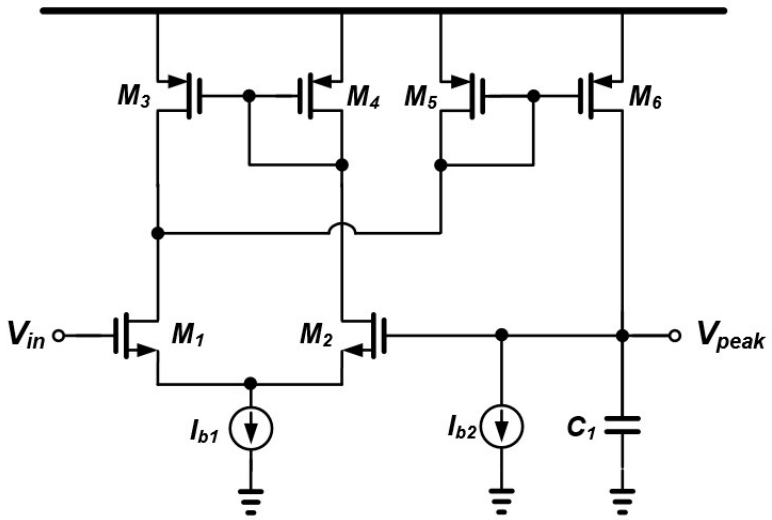
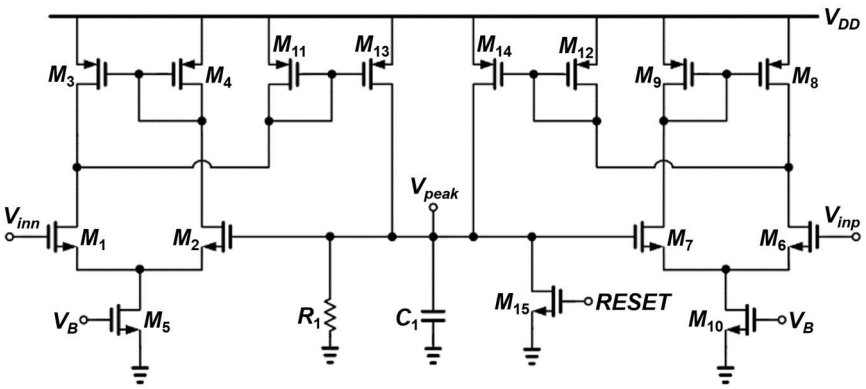


Figure 3.23 Positive peak detector using current mirror.

In designing an AGC loop, this droop rate should be carefully determined to meet the AGC settling requirement. In addition, parasitic capacitors should be considered to see if the leakage current can affect the droop rate. A low droop rate peak detector could discharge slowly while the envelope of an input signal keeps decreasing faster below the previous peak voltage, in which case the V_{peak} cannot follow the V_{in} fast enough. Thus, we need to reset the peak detector periodically so that it can quickly follow the next input peak point. A reset mechanism can be implemented with a simple NMOS switch across the hold capacitor C_1 which zeros the output instantly.

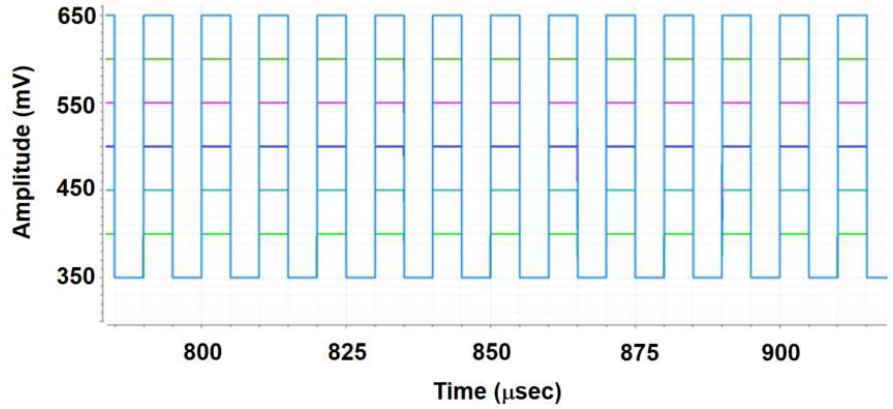
As shown in Fig. 3. 23, a positive peak detector is constructed with a differential amplifier ($M_1 \sim M_4$) and a current mirror (M_5 and M_6). If the V_{in} is larger than V_{peak}, the excess current is flowing through M_5 which is also copied to M_6 and charging the hold capacitor C_1. The small current source I_{b2} is for discharging. We can control the droop rate of the peak detector by adjusting the values of capacitance and the current source.

Fig. 3.24 shows design of a peak detector in proposed receiver in which is a differential version of the positive peak detector using current mirror in Fig. 3.23. Both positive

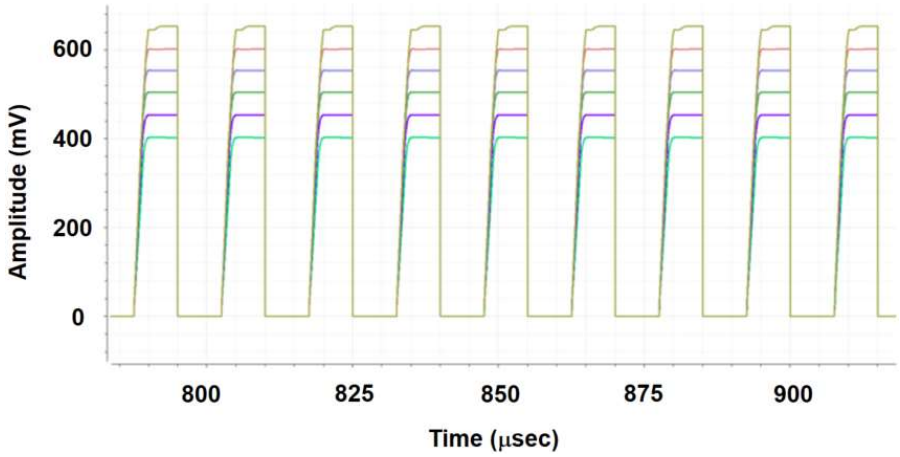


M_1, M_2, M_6, M_7	10 µm / 1 µm	M_3, M_4, M_8, M_9	6 µm / 5 µm	M_{11}, M_{12}, M_{13}, M_{14}	6 µm / 5 µm
M_5, M_{10}	4 µm / 8 µm	R_1	500 kΩ	C_1	1.79 pF

Figure 3.24 Schematic of a peak detector



(b)



(c)

Figure 3.25 Simulation results (a) input (b) output.

and negative differential input signals are fed to two identical positive peak detectors. The positive peak detector is implemented using differential amplifiers (M_1~M_{10}), current mirrors (M_{11}~M_{14}), and a low-pass filtering load (R_1, C_1, and M_{15}). If V_{in} is larger than V_{peak}, the excess current flows through M_{11}, M_{12} and is copied to M_{13}, M_{14}, charging the C_1, which holds the peak value. The R_1 provides a small amount of discharging current, and the M_{15} is used for resetting C_1. The droop rate of the peak detector can be controlled by adjusting the values of C_1 and R_1.

Fig.3.25 (a) and (b) show the simulation results of peak detector. When the input voltage peak is changed from 350mV to 650mV to 50mV step, the output voltage follows the input peaks.

3.3 Experimental Results

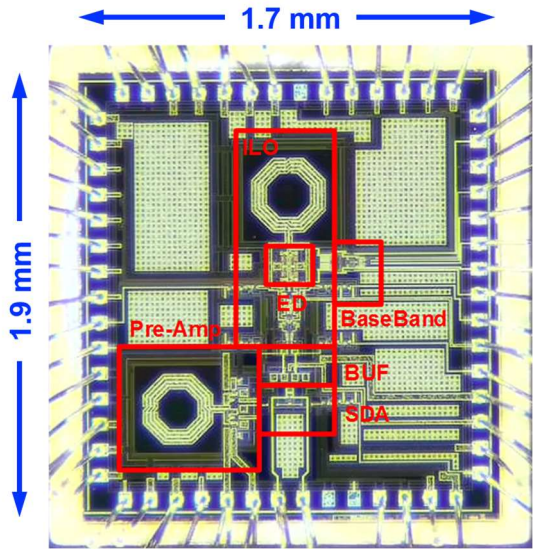
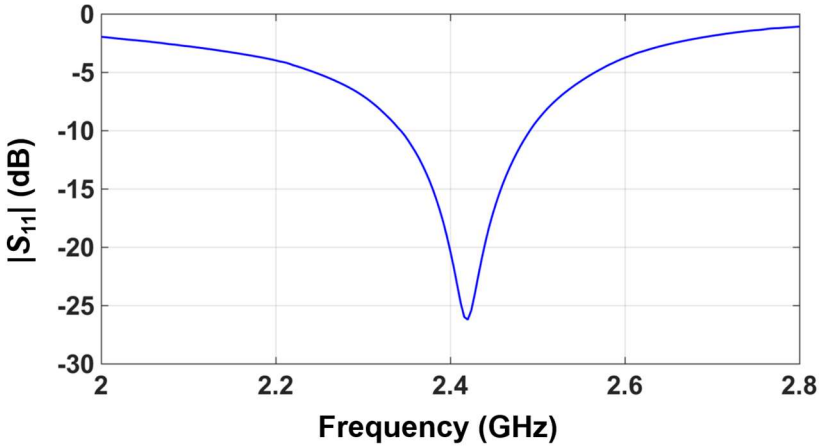


Figure 3.26 Chip micrograph of the fabricated receiver IC.

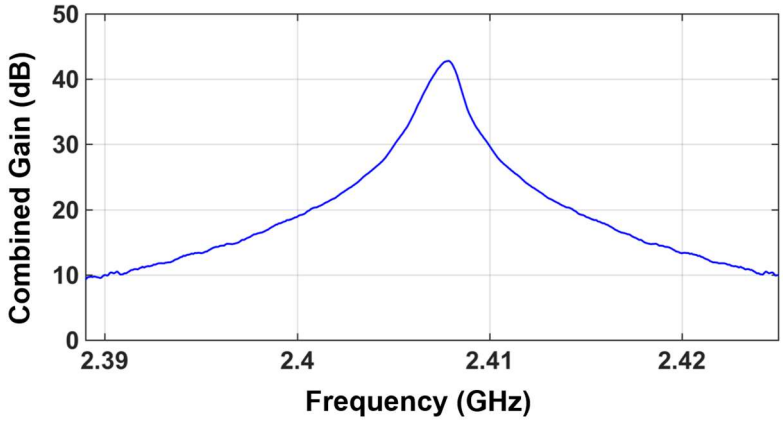
The proposed ILO-based OOK/BFSK/DBPSK receiver has been fabricated with 0.18-μm CMOS process technology, and the chip micrograph is shown in Fig. 3.26. The total chip area, including the bonding pads, is 1.7 mm × 1.9 mm. The receiver is implemented using three inductors. Two of them are the on-chip inductors used for the Pre-AMP and ILO, and the other is the off-chip inductor with high Q used for the SDA.

The input impedance matching characteristic of the receiver is shown in Fig. 3.27 (a), while the combined gain of the Pre-AMP and SDA is plotted in Fig. 3.27 (b) as a function of frequency. The magnitude of S_{11} is lower than –10 dB over the frequency range from 2.36 GHz to 2.49 GHz, which covers the ISM band. The Pre-AMP and Q-enhanced SDA provides a high voltage gain up to 43 dB with narrow bandwidth, which improves the sensitivity as well as the selectivity of the proposed receiver.

Fig. 3.28 shows the measured output waveforms of the ILO generated for the RF input signals with different modulation schemes. The baseband data of the input signal with a data



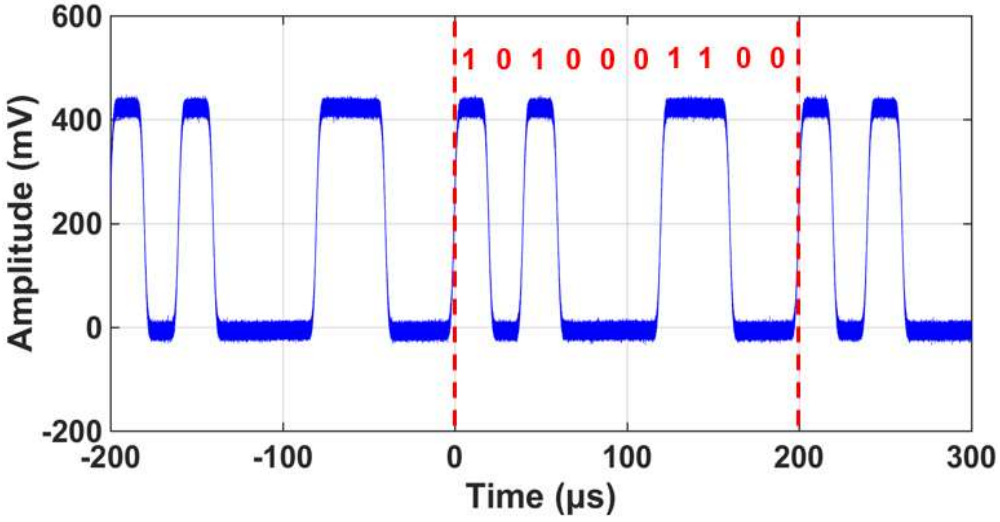
(a)



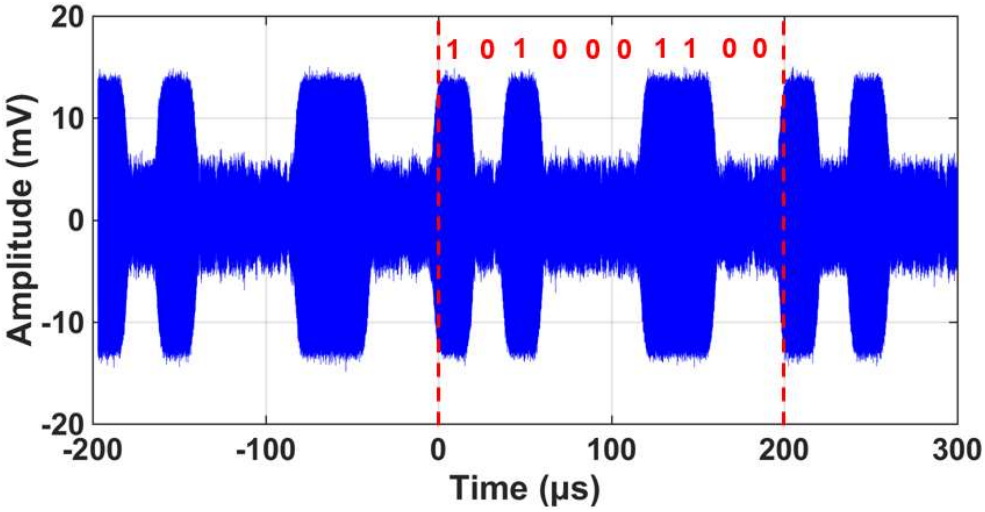
(b)

Figure 3.27 (a) Impedance matching characterisitc of the recever (b)Combined gain of the Pre-AMP and *Q*-enhanced SDA.

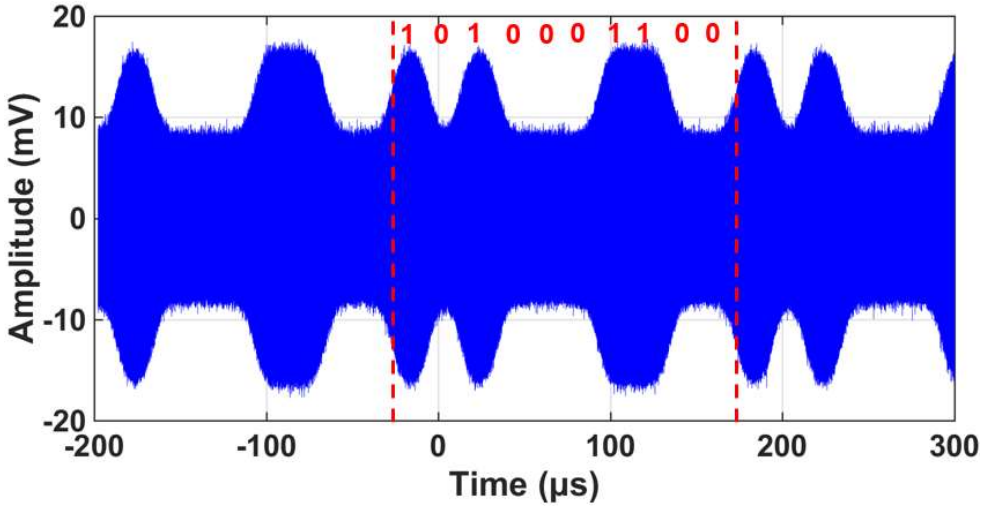
rate of 50 kb/s is shown in Fig. 3.28 (a). Based on this baseband data, –90-dBm RF input signals are generated with OOK, BFSK, and DBPSK modulation schemes. Fig. 3.28 (b) presents the output waveform of the ILO when the OOK-modulated input signal is applied to the receiver. As explained in Section III-D, the amplitude variations of the OOK-modulated input signal are preserved at the ILO output, and thus the amplitude of the ILO output signal varies according to the input baseband data. Fig. 3.28 (c) shows the output waveform of the ILO when the receiver input is the BFSK signal modulated between 2.404 GHz and 2.406 GHz with the frequency deviation of 2 MHz. The frequency-to-amplitude


1 0 1 0 0 0 1 1 0 0
Amplitude (mV)
Time (μs)

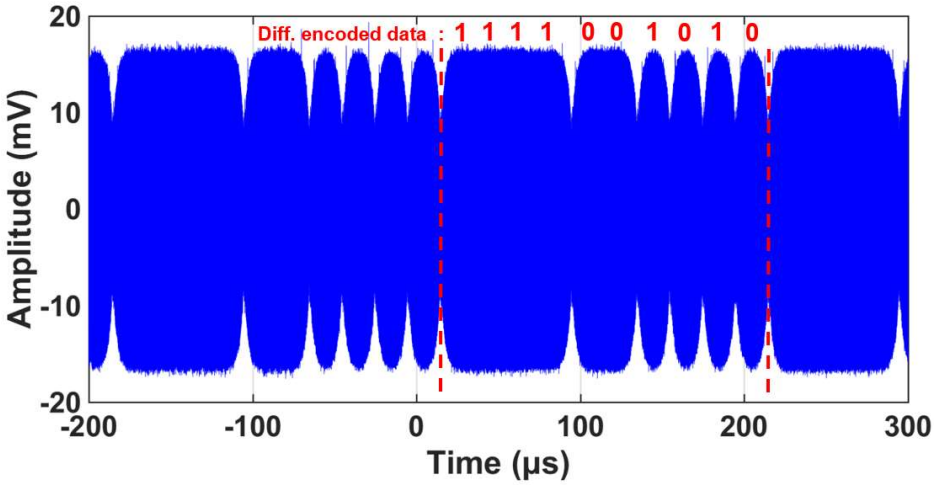
(a)


1 0 1 0 0 0 1 1 0 0
Amplitude (mV)
Time (μs)

(b)


1 0 1 0 0 0 1 1 0 0
Amplitude (mV)
Time (μs)

(c)



(d)

Figure 3.28 (a) Baseband data of the receiver input and the corresponding ILO output waveforms for the receiver input modulated by (b) OOK, (c) BFSK, and (d) DBPSK schemes.

conversion characteristic of the ILO generates the variations in the amplitude of the ILO output signal corresponding to the input baseband data. The ILO output waveform for the DBPSK-modulated input signal is shown in Fig. 3.28 (d). When the phase of the input signal changes, the ILO is perturbed from its injection-locked state, resulting in the instantaneous change of the ILO output amplitude. After the transient amplitude fluctuation, the ILO turns back to the injection-locked state, and its original output amplitude is recovered. It is found that the ILO output waveform presents an RZ signal characteristic as explained in Section III-C, and therefore the input baseband data can be recovered by converting the RZ signal to the NRZ data. From the results shown in Fig. 3.28, it is verified that the OOK/BFSK/DBPSK-modulated input signal can be converted to the amplitude-modulated output signal by the ILO operation, which enables the energy-efficient ED-based receiver structure.

As illustrated in Fig. 3.1, the ILO output is fed to the ED to generate the baseband signal capturing the variations in the amplitude envelope of the ILO output, and the ED output is

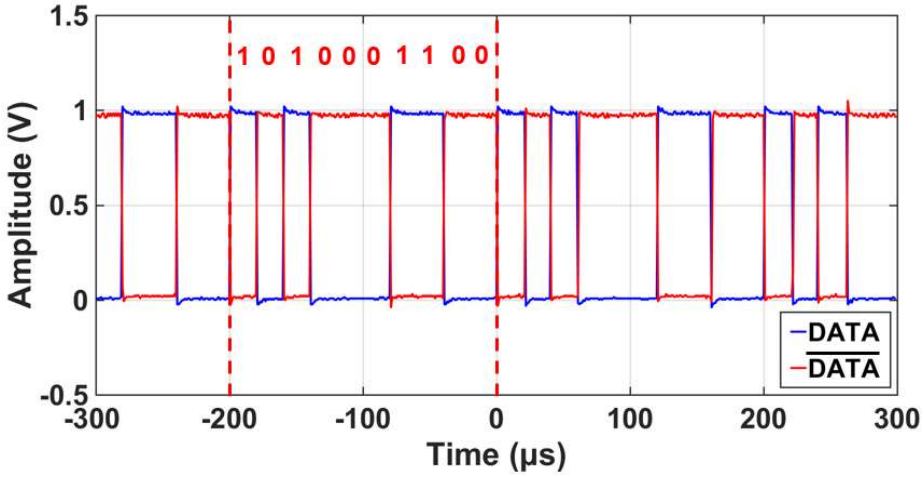


Figure 3.29 Demodulated output data of the receiver.

amplified by the BB AMP. The amplified baseband signal is processed by the comparator to produce the output bit stream.

Note that the output of the ED is AC-coupled to the input of the BB AMP. When the receiver input signal is OOK- or BFSK-modulated, the comparator output can directly be used as the demodulated output data. In the case of the DBPSK-modulated input signal, the comparator output needs to go through the conversion process from the RZ data to the NRZ data to produce the demodulated output. Fig. 3.29 presents the demodulated output of the receiver, which is consistent with the input baseband data shown in Fig. 3.28 (a). This result verifies that the proposed receiver can process the modulated RF input signal properly to generate the correct and accurate output data.

When the RF input signal is BFSK-modulated, as shown in Fig. 3.1 and discussed in Chapter II, the peak detector is used to regulate the strength of the ILO injection signal so that the frequency-to-amplitude conversion performance of the ILO can be maintained reliably. The peak detector provides the amplitude information of the baseband signal to the MCU through the analog-to-digital converter (ADC) interface of the MCU, and the MCU

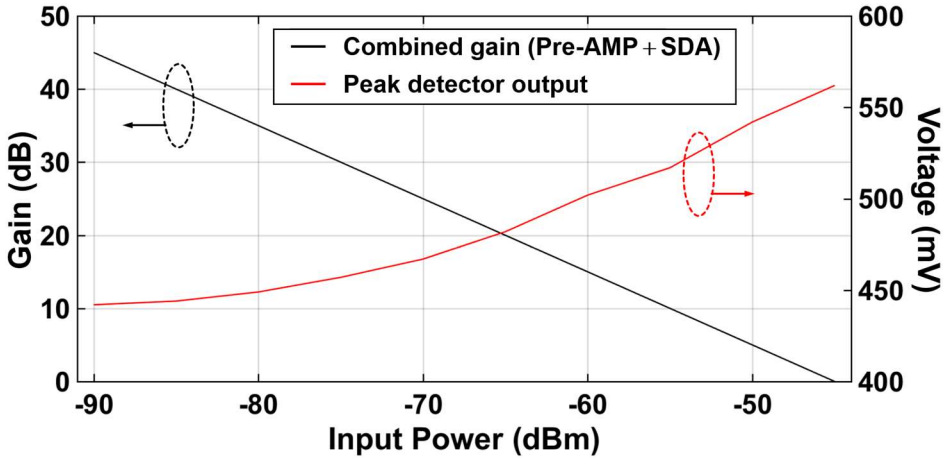
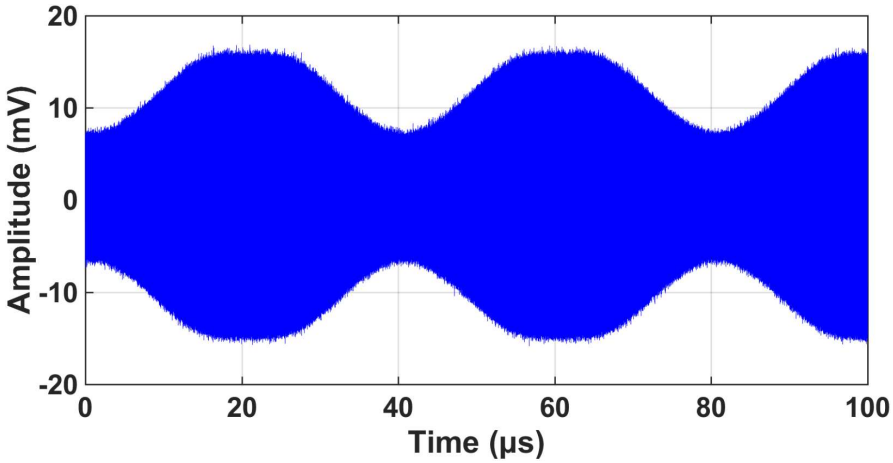


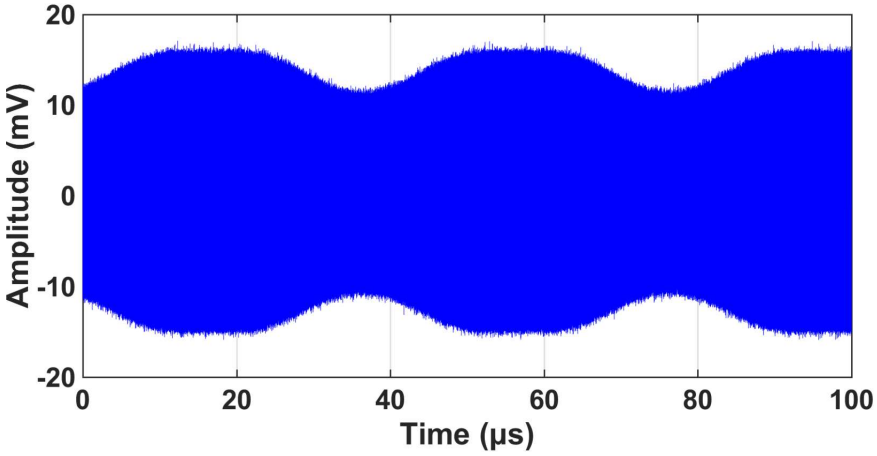
Figure 3.30 SDA gain control characteristic as a function of the receiver input power.

generates an appropriate DC voltage (V_{CTRL} in Fig. 11) through its DAC output to control the SDA gain, forming the closed regulation loop. In the proposed receiver, the amplitude of the ILO injection signal is kept constant at –45 dBm to obtain the lock range of about 2 MHz consistently, leading to an optimal frequency-to-amplitude conversion ratio. As shown in Fig. 3.30, when the receiver input power changes from –90 dBm to –45 dBm, the peak detector generates the corresponding output voltage varying from 440 mV to 560 mV, and this information is processed by the external MCU to control the SDA gain from 45 dB to 0 dB. As a result, the ILO injection strength is regulated to –45 dBm for the wide range of the receiver input power.

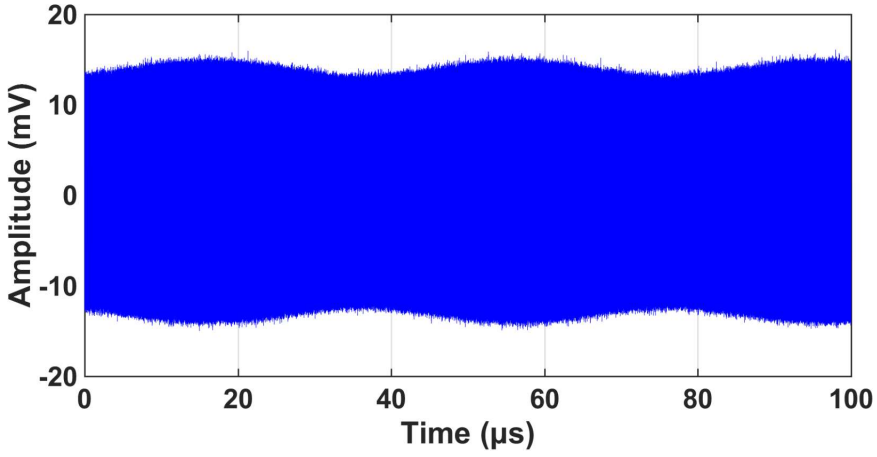
Fig. 3.31 shows the ILO output waveform for different levels of the receiver input power when the closed-loop SDA gain control function is disabled, and the combined gain of the Pre-AMP and SDA is fixed at 25 dB. As shown in Fig. 3.31 (a), if the RF input signal is FSK-modulated with the frequency deviation of 2 MHz and its power level is –70 dBm, the ILO output exhibits a sufficiently large amplitude variation of 8 mV. However, as the power of the input signal increases, the frequency-to-amplitude conversion ratio degrades greatly,



(a)



(b)



(c)

Figure 3.31 ILO output waveforms measured for the BFSK-modulated receiver input signal with different power levels: (a) –70 dBm, (b) –66 dBm, and (c) –64 dBm, when the SDA gain control loop is disabled.

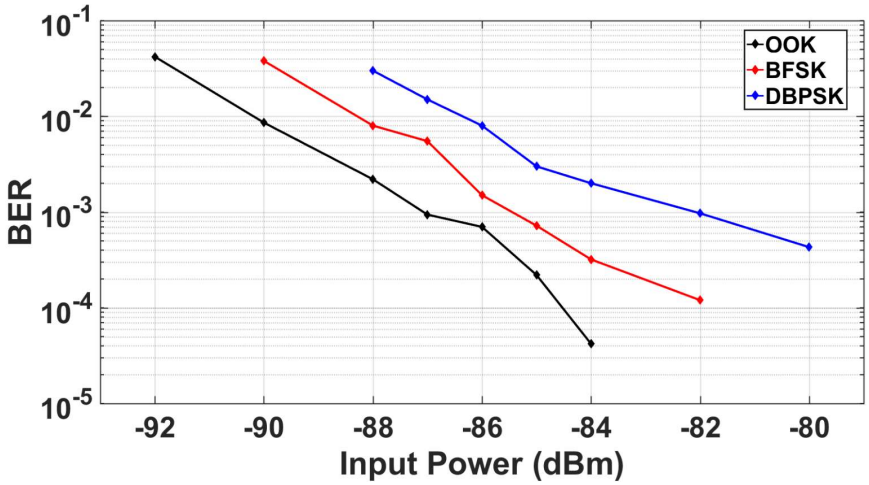


Figure 3.32 BER performance of the proposed receiver measured with the data rate of 50 kb/s as a function of the input power.

as shown in Fig. 3.31 (b) and (c). This result demonstrates the importance of regulating the power of the ILO injection signal through the closed-loop gain control.

Fig. 3.32 plots the bit-error-rate (BER) test results performed at the data rate of 50 kb/s with varying the receiver input power.

It is found that the proposed receiver achieves the sensitivity of –87, –85, and –82 dBm when the input is modulated with OOK, BFSK, and DBPSK schemes respectively for the data rate of 50 kb/s and BER of 10^{-3}. The signal-to-interference ratio (SIR) performance measured for the interferer near the 2.4-GHz ISM band is presented in Fig. 3.33. For this SIR measurement, the data rate is set to 50 kb/s, and the input signal power is adjusted to be 6-dB higher than the sensitivity limit of the receiver. The measurement is repeated for different modulation schemes. The SIR measurement result indicates the power level of the interferer that the receiver can withstand. Typically, the ILO-based receiver is vulnerable to the blocker because the ILO can be locked erroneously to the interferer. However, as shown in Fig. 3.33, the proposed receiver can mitigate this issue significantly by employing the *Q*-

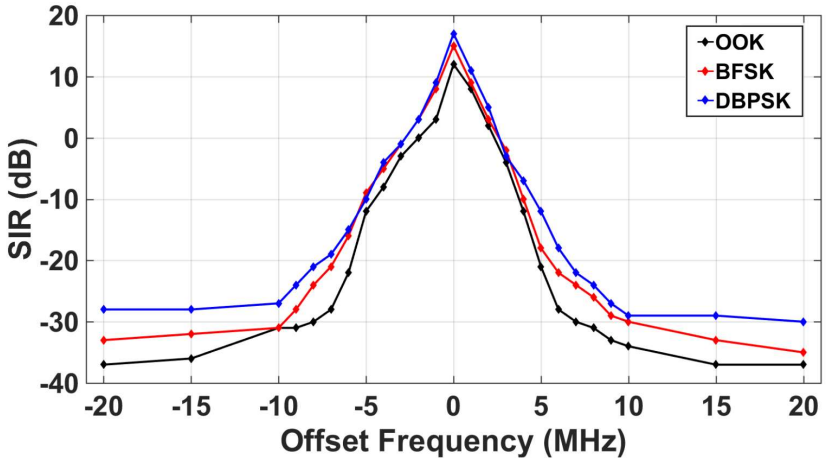


Figure 3.33 SIR performance of the proposed receiver measured with the data rate of 50 kb/s and the 6-dB higher input power than the sensitivity limit.

Table 3.1 Power Breakdown of the Receiver

Pre-Amplifier	75 μA
SDA	33 μA
Buffer	80 μA
ILO	130 μA
ED	2 μA
BB AMP	2 μA
Comparator	1 μA
Peak Detector	1 μA
Total Power	324 μW

enhanced SDA with the narrow-band amplification characteristic. The measurement results verify that the receiver can distinguish the input signal from the accompanying interferer, exhibiting good selectivity performance. The power breakdown of the receiver is shown in Table 3.1. The total power consumption is 324 μW when operated with the supply voltage

Table 3.2 Performance Summary and Comparison with Previous Works

	[5]	[7]	[9]	[16]	[22]		[23]	This work
Technology (nm)	65	90	180	130	65		40	180
Supply Voltage (V)	0.6	0.5	0.7	0.7	0.6		0.65	1
Architecture	Low IF	Uncertain IF	Injection Locking	Envelope Detection	Sliding IF		Super Regeneration	Injection Locking
Frequency (MHz)	2400	2000	920	915	2400		900	2400
Modulation	OOK	OOK	BFSK	BFSK	BFSK		OOK	OOK/BFSK/DBPSK
Data Rate (kb/s)	1000	100	5000	500	25	1000	50	50
Sensitivity (dBm)	-83	-72	-73	-90	-102	-86	-87	-87
Power consumption (μW)	227	52	420	500	466		320	324

of 1 V. The most of power is consumed by the Pre-AMP, SDA, buffer, and ILO, while the consumption by the ED, BB AMP, comparator, and peak detector is nearly negligible. Table 3.2 summarizes the key performances of the proposed receiver and compares them with those of other recent low-power receivers. The receiver presented in this work exhibits competitive performances when compared with other designs. Especially, the proposed receiver can operate with multiple modulation schemes and improves the previous injection-locking-based receiver [9] in that the strength of the injection signal to the ILO is controlled in a closed-loop manner, guaranteeing consistently good performances over a wide range of the receiver input power.

3.4 Summary

In this chapter, the ultra-low power receiver supporting OOK/BFSK/DPSK multi-modulation is designed that operates in the 2.4GHz ISM band. The amplitude, frequency, phase to amplitude-modulated signal conversion of the injection-locked LC oscillator to an enables the implementation of an envelope detector based receiver typically used in low power receivers. Through the high voltage gain using the Q-enhancement technic of SDA, the input signal amplitude that is enough for injection locking is obtained and achieve a high sensitivity.

The injection locked LC oscillator, a key component of the RF front-end, is designed and implemented as a complementary negative resistor structure to reduce power consumption. In the case of the BFSK modulation, the lock range varies according to the strength of the input signal, and the demodulation performance of the receiver is eventually deteriorate because the frequency to amplitude conversion ratio cannot be kept constant. In order to prevent performance degradation, an external automatic gain control loop is placed in the receiver. In the future, the integration level can be increased by designing an internal automatic gain control loop.

The receiver implemented in this chapter has the disadvantage that it requires a larger input for injection locking, but the technic to amplify the input signal sufficiently such as Q-enhancement is applied, the receiver structure based on the injection lock LC oscillator is suitable for a high-performance low-power receiver compare with conventional receivers discussed in Chapter I.

IV. Ultra-low Power GFSK Demodulator Based on an Injection Locked Ring Oscillator

Gaussian frequency shift keying (GFSK) is a popular modulation scheme for short-range, multi-channel communication standards such as Bluetooth and WPAN due to its high sensitivity and superior spectral efficiency [24]. Several GFSK transceivers have been actively developed in order to implement a physical layer for wireless networks [25]. The demand for GFSK transceivers having small feature sizes and lower power consumption has increased in recent Internet-of-Things (IoT) and Medical Implanted Communication Service (MICS) applications.

Consequently, research efforts have been focused on reducing the feature size as well as the power consumption of such transceivers [26], [27]. GFSK transmitters can be power-efficient, as the constant envelope characteristics of the GFSK modulation allow the use of energy-efficient nonlinear power amplifiers, enabling a low-power operation without any data distortion caused by spectral regrowth [28]. However, conventionally, GFSK receivers have a complicated structure and consume larger power.

Secondly, they tend to have a large size, limiting their suitability for such size-constrained and low-power applications. To address these problems, the zero-IF and low-IF architectural flavors that integrate all filter components to a single chip are commonly used in the GFSK receivers [29]. However, the zero-IF has intrinsic issues caused by flicker noise and DC offset as well as local oscillator leakage. As a result, the low-IF is a more preferred option for enhanced signal-to-noise ratio (SNR) performance. Nevertheless, the low-IF receivers still suffer from relatively low energy efficiency due to

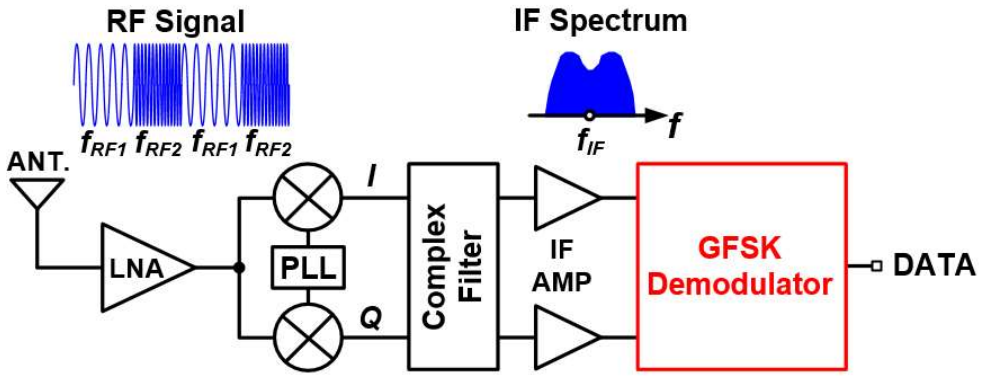


Figure 4.1 Overall structure of a GFSK receiver with a low IF.

the high frequency operation needed in detecting two different IF frequencies during the demodulation process. Therefore, in this paper, we present an ultra-low power, low cost demodulator for the GFSK receivers with a low IF that can improve the energy efficiency by more than 30 times than those of the recently presented works [30-33].

Several GFSK demodulators employing techniques such as delay line discrimination [30], zero-crossing detection [31], phase domain analog-to-digital conversion [32], and FM discrimination [33] have been reported in prior literature. The delay line discrimination approach of [30] is complex and consumes large power of about 200 μW as it uses two voltage-controlled delay loops for its operation. Similarly, the zero-crossing technique used in [31] also has a limited suitability for low power operation as it uses a Sallen-Key filter and a differentiator whose power consumptions are 270 μW and 180 μW respectively. The demodulator based on the phase domain analog-to-digital converter in [32] needs several current mirrors and comparators and thus inevitably consumes over 500 μW. The last structure with the FM discriminator [33] still consumes large power of 170 μW due to the high sampling frequency of 32 MHz. Thus, the recent demodulators for the GFSK receivers are less suitable to be employed in low power sensor nodes or in bio-medical applications. To solve the above-mentioned problems regarding area and power consumption, we

propose an injection locked ring oscillator (ILRO) based GFSK demodulator. Section 4.1 presents the proposed demodulator architecture employing an ILRO and discusses the detailed circuits of pulse slice and ILRO in the demodulator. Section 4.2 presents the chip measurement results before summary of Section 4.3.

4.1 Overall Demodulator Architecture

The architecture of GFSK receivers using a low IF scheme is shown in Fig. 4.1. It comprises a low noise amplifier, mixers, a local oscillator, a complex filter, IF amplifiers as well as a demodulator. The RF front-end amplifies and down converts the RF input to the IF signal. The image components from the IF signal are filtered out by the complex filter, and the digital data is recovered by the demodulator. Among the various blocks of a GFSK receiver, the demodulator is one of the components that dissipate significant power and hence, minimizing it is essential in improving the overall power efficiency [31]. This paper proposes an ultra-low power, low cost GFSK demodulator using an ILRO towards achieving this end.

The proposed GFSK demodulator based on an ILRO is shown in Fig. 4.2. The input signal is down-converted to IF signal (A). The frequency f_{IF1} represents a data bit '1' while the frequency f_{IF2} represents a data bit '0'. The signal A is passed through a limiter to obtain B, which has a constant voltage swing. The pulse slicer generates an approximately 25%-width pulse output C that serves as the injection signal to the ILRO from its input B. The ILRO, once locked, maintains the phase differences between the injection input C and its output D such that C will always lead or lag D when the modulator input frequencies

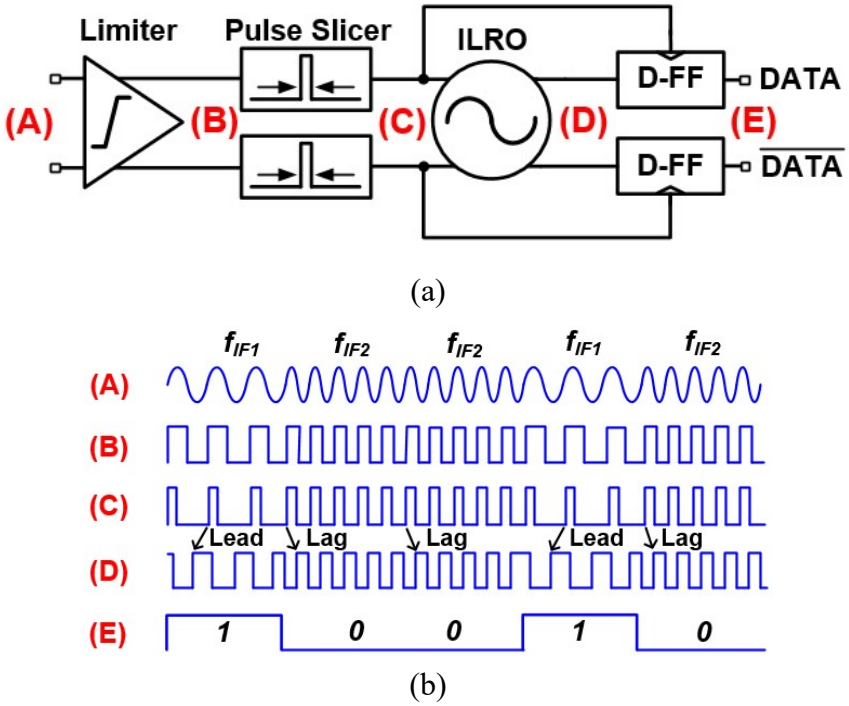


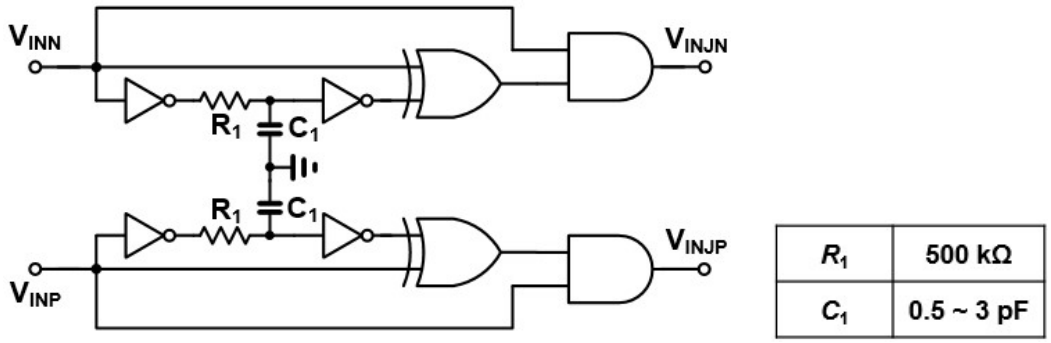
Figure 4.2. Block diagram and timing waveforms of the proposed ILRO based GFSK demodulator.

are f_{IF1} and f_{IF2} respectively. The demodulator frequency has to be chosen to strike a balance between power consumption and the transient settling time of the ILRO to get to a locked state. For this reason, 2 MHz was selected for the design goal of power consumption under 3 μW and 500 kbps data-rate.

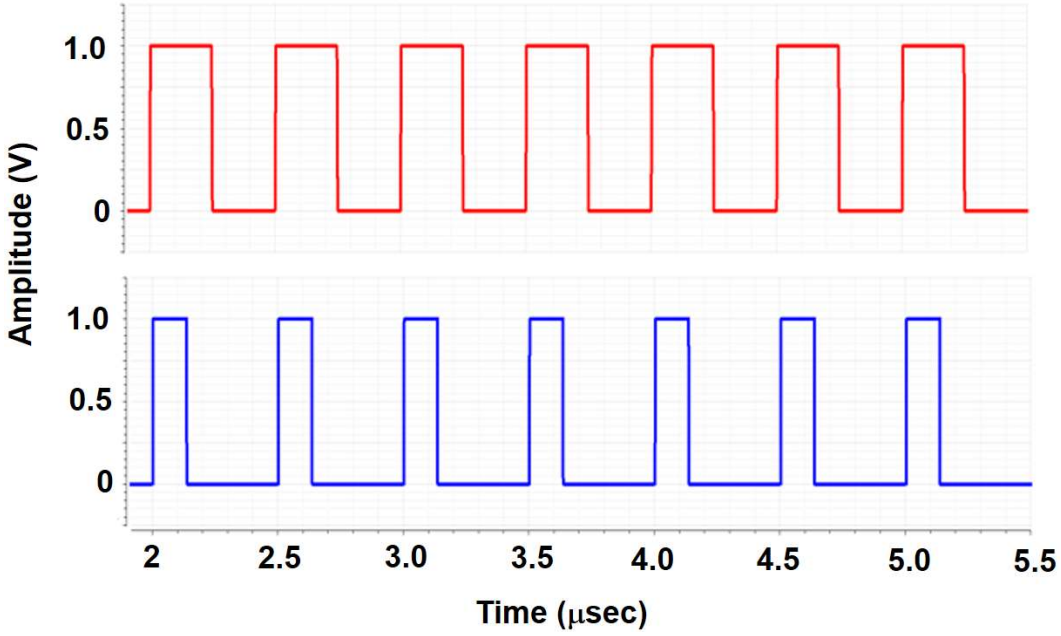
The flip-flop (DFF) serves as a 1-bit time-to-digital converter that samples the ILRO output D during the rising edge of the injection pulse C. Given the fixed lead/lag relationships between C and D established by the ILRO, the input data can be reliably demodulated by this approach as D will sample a logic high from the signal C when the input frequency is f_{IF1} and a logic low when the input frequency is f_{IF2}. In comparison to conventional demodulators, the proposed architecture is simple and digital-intensive while the overall power consumption is significantly lower than conventional approaches that uses analog methods.

4.2 Details of the Blocks

4.1.1 Pulse Slicer



(a)



(b)

Figure 4.3 Pulse slicer (a)schematic (b)input and output waveform.

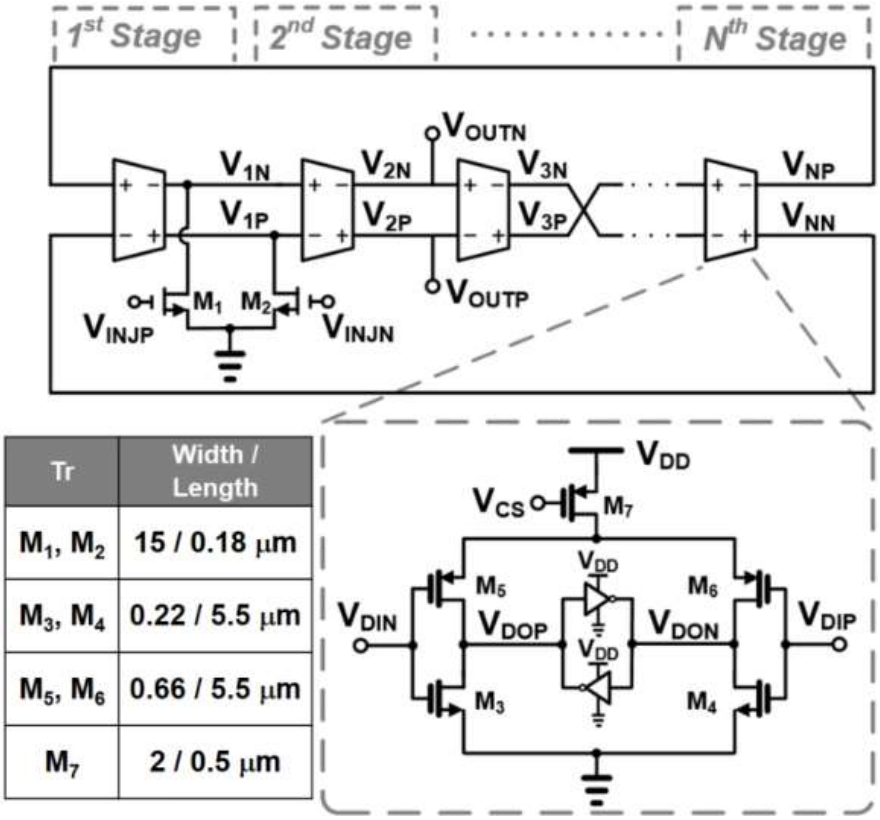
The schematic of the pulse slicer used in the GFSK demodulator is shown in Fig. 4.3 (a). The pulse slicer makes the pulse-width of the ILRO injection signal approximately equal to the time constant R_1C_1, designed such that the pulse slicer output width is ~25 %

of that of the free-running ILRO output. The output pulse width is tuned to the target value by controlling the capacitor banks C_1. The reason for using the 25% duty-cycle is explained in Chapter II. The pulse slicer input and a delayed version of the same are passed through an XOR gate to generate pulses on both the rising and falling edges of the input. Only the pulse generated on the rising edge of the input goes to the output due to the AND operation. Fig. 4.3 (b) shows the simulation result of the pulse slicer. The input signal is set 2 MHz, which is the IF frequency of demodulator. When the C_1 value is 2 pF, the output pulse width of 25 % is obtained.

4.1.2 Injection Locked Ring Oscillator

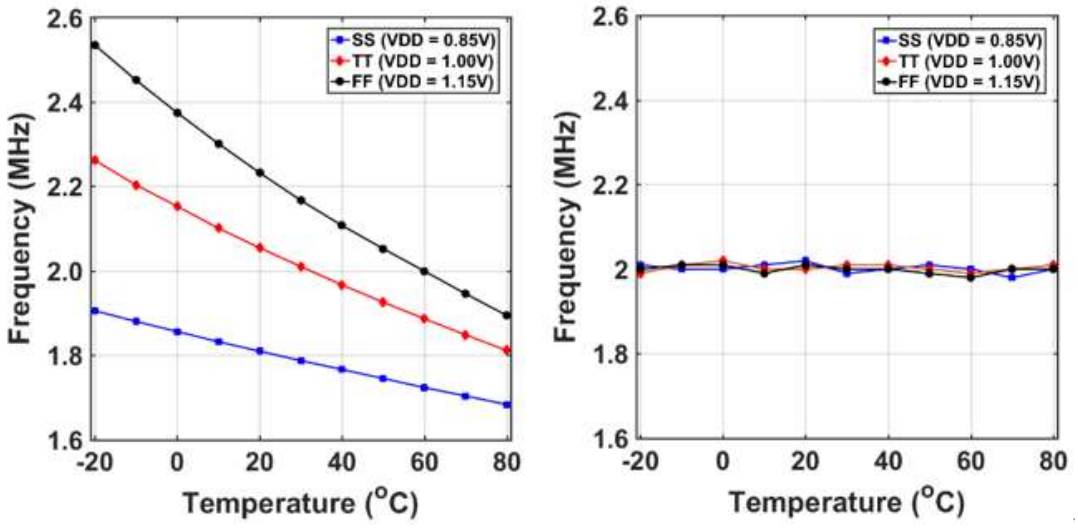
Fig. 4.4 shows the schematic of the differential N-stage ILRO used in the proposed GFSK demodulator. Note that we use a 4-stage ILRO (N=4) in this implementation. The injection signals V_{INJN} and V_{INJP} are complementally injected into the first nodes V_{1N} and V_{1P} by using NMOS switches. The phase-shifted outputs V_{OUTN} and V_{OUTP} are obtained from the nodes V_{2N} and V_{2P} respectively. The free running frequency of the ILRO is determined by the delay cell's PMOS current source bias V_{CS} as shown in Fig. 4.4. In addition, a latch circuit formed by cross-coupled inverters are added to the delay cells to minimize the rise/fall times of the ILRO node signals. The free-running frequency of ILRO is designed to 2 MHz. The ILRO used in the demodulator has 1.4 MHz (1.3 ~ 2.7 MHz) lock range.

The ILRO is vulnerable to PVT variation due to the open-loop operation. Deviation of the free-running frequency from the IF frequency of the receiver degrades the BER performance of the demodulator. Such effects can be minimized by using an external reference clock and a frequency locked loop (FLL) using a replica VCO as shown in Fig.



Tr	Width / Length
M_1, M_2	15 / 0.18 μm
M_3, M_4	0.22 / 5.5 μm
M_5, M_6	0.66 / 5.5 μm
M_7	2 / 0.5 μm

Figure 4.4 Schematic of the differential ILRO



(a) (b)

Figure 4.5 Change of free-running frequency of ILRO according to PVT (a) before calibration (b) after calibration

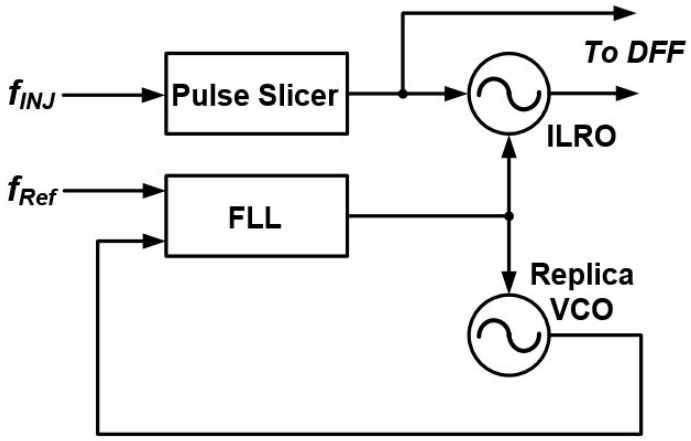


Figure 4.6 ILRO with frequency locked loop (FLL) using a replica VCO.

4.6 [34]. This implementation, however, does not include an on-line calibration circuit to mitigate the PVT effects. The free-running frequency of ILRO is tuned to the IF frequency used in the receiver by adjusting V_{CS}. Fig. 4.5 shows the change of ILRO's free-running frequency due to PVT variations and results of calibration. The free-running frequency of ILRO in proposed demodulator is changed from 1.7 to 2.55 MHz over a temperature and supply ranges of -20° C to 80° C and 0.85 V to 1.15 V respectively along with three different process corners, as shown in Fig. 4.5 (a). However, by adjusting V_{CS}, the free oscillation frequency can be moved closer to 2 MHz for various process corners such as FF (V_{DD}=1.15 V), TT (V_{DD}=1.0 V), SS (V_{DD}=0.85 V) as shown in Fig. 4.5 (b).

4.3 Experimental Results

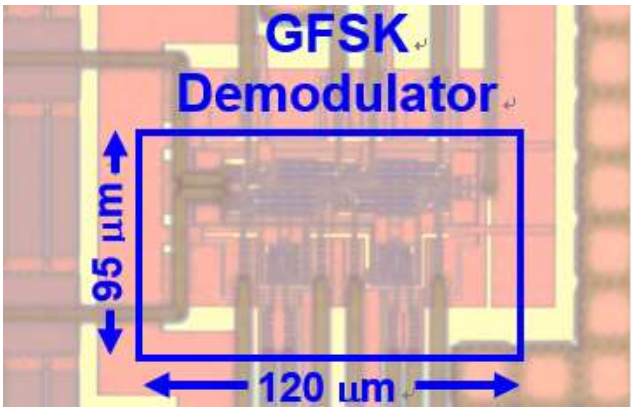


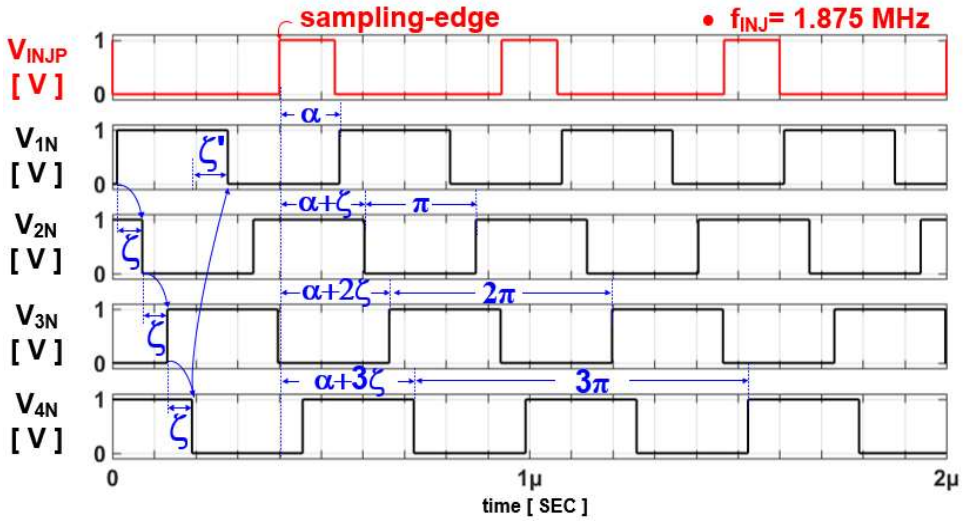
Figure 4.7 Chip micrograph of GFSK demodulator.

Table 4.1 Power Breakdown of the Demodulator

Limiter	220 nA
Pulse Slicer	560 nA
ILRO	1.5 μA
Latch	270 nA
DFF	150 nA
Total Power	**2.7 μW**

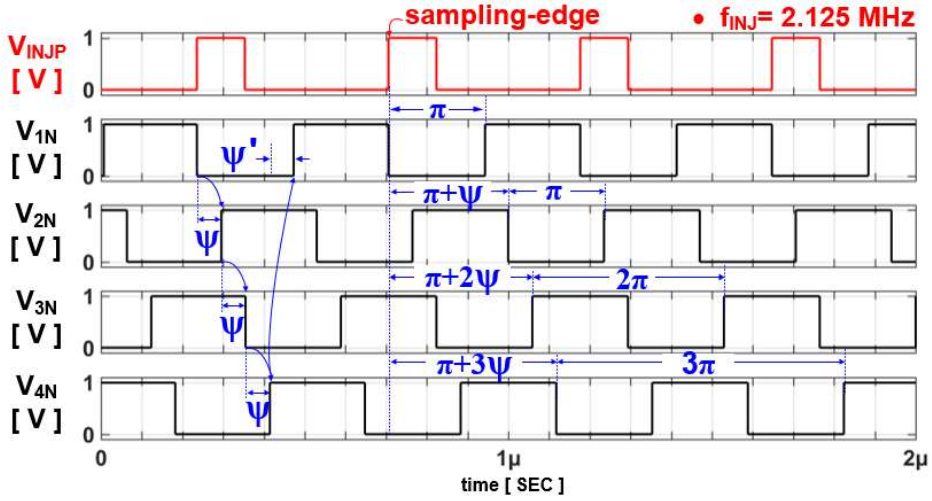
Fig. 4.7 shows the chip micrograph of the proposed GFSK demodulator. The demodulator is implemented in a 0.18 μm standard CMOS process and occupies an active area of 95 × 120 μm^2. The proposed demodulator consumes an average current of 2.7 μA from a 1.0 V supply. The power breakdown of the receiver is shown in Table 4.1. The most of power is consumed by the ILRO.

Fig. 4.8 shows the Cadence Spectre simulation results that plot the phase differences between injection signal and the output signal of each of the delay stages. The free-running



Parameter	ζ	ζ'	θ	ϕ	PD_2	Sampling state
Phase [°]	43.2	50.4	1.8	7.2	313.2	High

(a)



Parameter	ψ	ψ'	θ	ϕ	PD_2	Sampling state
Phase [°]	46.8	39.6	1.8	7.2	406.8	Low

(b)

Figure 4.8 Simulation results of 4-stage differential ILRO at $f_{INJ} < f_0$ (a) and $f_{INJ} > f_0$ (b).

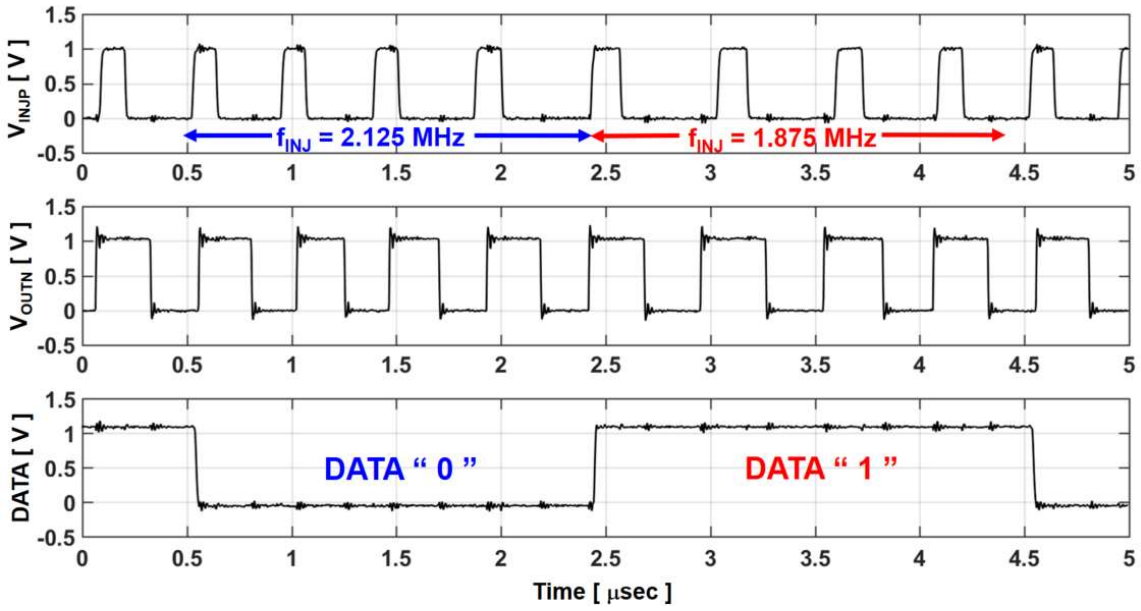


Figure 4.9 Measured GFSK demodulator responses.

frequency of ILRO is designed at 2 MHz and an approximately 25 % duty cycled injection signal is used. Fig. 4.8 (a) shows the output signal of each node in the injection locked state with the 1.875 MHz injection signal. From simulation, it can be seen that the phase shift of the delay cell has a phase shift ζ is 43.2° and ζ' is 50.4°. Thus, the values θ and ϕ can be evaluated as 1.8° and 7.2° respectively. When ILRO is locked to the 2.125 MHz signal as shown in Fig. 4.8 (b), the phase shift ψ is 46.8° and ψ' is 39.6°. In this case also, the values θ and ϕ can be evaluated as 1.8° and 7.2° respectively as expected from (2.19), (2.20) and (2.27). In this implementation, the outputs are taken from the second stage delay cells. When the injection frequency is lower than the free-running frequency, based on the simulation results, the phase difference of the second delay cell output and the injection signal is 313.2° from (2.34). In other words, the rising edge of second stage delay cell output is 46.8° ahead of the sampling edge of V_{INJP}. Since PD_2 is lower than 360° (or 2π), the output is sampled as logic-high. When the injection frequency is higher than free-running frequency, the phase difference PD_2 is 406.8° from (2.35). The rising edge of

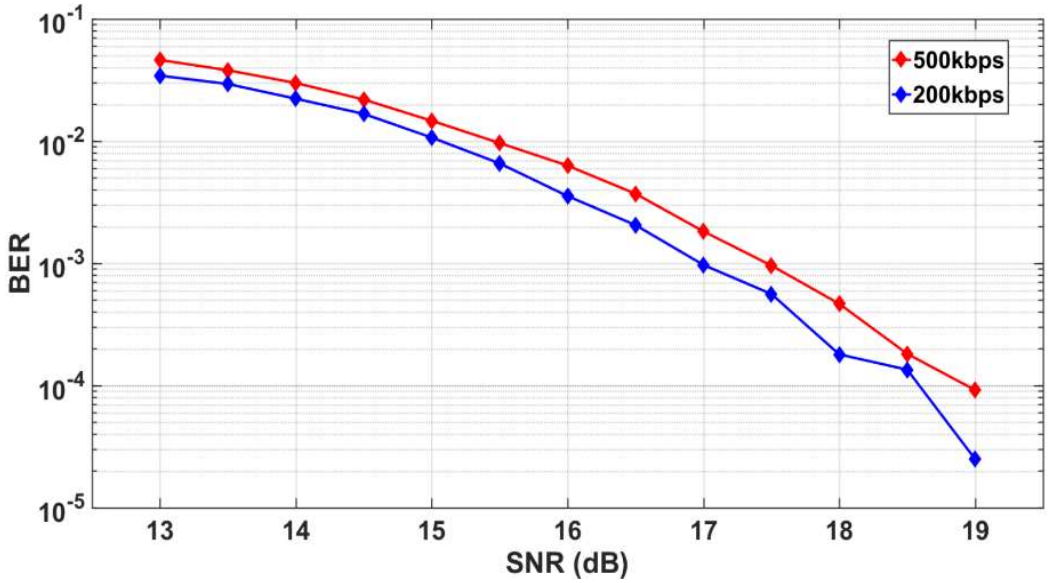


Figure 4.10 Measured BER performances of the GFSK demodulator.

second stage delay cell output is 46.8° lag to V_{INJP}. Since PD_2 is higher than 360° (or 2π), the output is sampled as logic-low.

Fig. 4.9 shows the measured input and output waveforms of the ILRO in the proposed demodulator and the data waveform demodulated through the D-flip flop using and injection signal of 25 % duty cycle. It can be seen that when the injection frequency is 2.125 MHz, the output is sampled as a logic-low. Similarly, when the injection frequency is 1.875 MHz, the output is sampled as a logic-high. In order to measure the BER performance, GFSK signal with AWGN (Additive White Gaussian Noise) and frequency deviation of ±125 kHz is applied to the demodulator by using signal generator, SMW200A of ROHDE & SCHWARZ. As shown in Fig. 4.10, the demodulator achieves an input SNR of 17.5 dB equivalent to a BER of 0.1 % at a data rate of 500 kbps. At 200 kbps, the SNR improves to 16.9 dB.

Table 4.2 compares the performance of recently proposed GFSK demodulators with the proposed architecture. In comparison to [27]-[30] the proposed demodulator consumes significantly lesser power achieving energy efficiency at least 30 times better. The overall

Table 4.2 Performance Comparison

	[30]	[31]	[32]	[33]	This work
Tech [μm]	0.18	0.18	0.18	0.13	0.18
Supply [V]	0.5	1.8	1.8	1.2	1.0
Max. Data-rate [Mbps]	1	1	0.25	1	0.5
IF [MHz]	3	3	2	1	2
SNR [dB]	18.7	16.5	16.7	14.4	17.5 @ 0.5 kbps 16.9 @ 0.2 kbps
Power [μW]	200	918	630	170	2.7
Energy Efficiency [pJ/bit]	200	918	2520	170	5.4
Area [mm^2]	0.36	0.08	0.14	0.05	0.012

silicon area is 4 times smaller, thanks to its simple structure arising from the ILRO based approach. The energy efficiency and the area can be further improved by implementing the proposed modulator in a more advanced process node due to its digital intensive nature.

4.4 Summary

In order to design a high performance receiver, the conventional low-IF structure is widely used, but due to the complexity and high power consumption, it was difficult to implement a low power receiver.

Not only the power consumption of the RF front end and LO generation of the receiver, but also the power consumption of the demodulator is one of the challenges to be solved in the implementation of the low-IF structure. The demodulators of various structures previously published have high complexity and high power consumption compared with the proposed demodulator.

In this chapter, the GFSK demodulator for a low-IF receiver is designed and implemented using the frequency phase conversion characteristics of ILRO that described in Chapter II. Through the pulse slicer of the input stage, the phase lead or lag between the input and output of ILRO occurs according to the input frequency, and data can be easily restored through DFF. As the simple and ultra-low power demodulator based on ILRO proposed in this chapter is applied to the Low-IF receiver in the future, the total power consumption of receiver can be greatly reduced.

Although the open-loop operation of ILRO shows a susceptible to PVT variation, when the proposed demodulator is applied to the receiver, it can be overcome by adding a feedback loop of replica-VCO. In addition, as the amount of lead or lag of the phase can be accurately discriminated, it is available to extend a QFSK demodulator.

V. Conclusion

A wireless receiver is one of the most important block in the wireless sensor node for IoT. Current market demands and trends in the electronics industry suggest that communication devices need to support lower power consumption and higher performance. The conventional receiver structures such as direct conversion and heterodyne have high performance but these structures cannot operate in low power. The previously published low power receiver using OOK modulation cannot achieve high sensitivity and channel selectivity. To address these disadvantages, in this thesis, we propose the ultra-low power receiver based on injection locked LC oscillator that is a key building block in the proposed receiver. Furthermore, the ultra-low power demodulator based on injection locked ring oscillator also is proposed and implemented for decreasing power consumption of low-IF receiver for IoT.

First, an injection locked LC and Ring oscillator that are core blocks of proposed receiver and demodulator are theoretically analyzed in this thesis, resulting in a better understanding of injection locking phenomenon. The injection locked LC oscillator can be used in receiver supporting multiple modulation schemes such as OOK, BFSK, DPSK due to amplitude, frequency, phase to amplitude conversion properties. The amplitude modulated signal allows to use simple envelope detection for demodulation and down conversion.

The injection locked ring oscillator also have frequency to phase conversion property that used in proposed demodulator. It allows to simple structure and ultra-low power operation. A DFF only need for a frequency discrimination because of the frequency to phase conversion in the injection locked ring oscillator.

By using the injection locked LC oscillator, an energy-efficient multi-mode receiver that operates in the 2.4-GHz ISM band is presented for use in the wireless sensor node under various IoT application scenarios. The ILO is at the core of the receiver structure, and its inherent injection-locking characteristic is exploited to convert the amplitude, frequency, and phase variations of the OOK, BFSK, and DBPSK input signals respectively to the amplitude fluctuations at the ILO output. After this conversion process, a simple envelope detection follows to extract the amplitude variations of the ILO output envelope as well as to down-convert the signal to the baseband. Consequently, the use of the mixer and the frequency synthesizer can be excluded to minimize the power consumption.

Importantly, the proposed receiver implements the closed-loop control of the ILO injection signal power, unlike the previous ILO-based FSK receiver. The control loop operates by adjusting the *Q*-enhanced SDA gain according to the baseband signal power monitored by the peak detector.

Without this loop, as the receiver input power increases, the ILO lock range becomes wider, and the frequency-to-amplitude conversion performance degrades, leading to the demodulation failure eventually.

In the RF front-end, the Pre-aMP and *Q*-enhanced SDA are employed to provide a sufficiently large differential injection signal to the ILO even when the RF input power is low, which improves the receiver sensitivity significantly. In addition, the receiver selectivity is also improved due to the narrow-band amplification characteristic of the *Q*-enhanced SDA.

When fabricated in 0.18-μm CMOS technology, the proposed receiver achieves the sensitivity of –87, –85, and –82 dBm for the OOK, BFSK, and DBPSK signals respectively

at the data rate of 50 kb/s and the BER lower than 0.1 % while consuming 324 μW from the 1-V supply.

The future work targets on designing an internal auto gain control loop for high integration level. In addition, to decrease more operating power, a duty cycling and a wake-up receiver can be employed in the proposed receiver.

In this thesis, also, a novel GFSK demodulator based on an injection ring oscillator suitable for low-IF receiver architecture is presented. The GFSK demodulator for a low-IF receiver is designed and implemented using the frequency phase conversion characteristics of ILRO. Through the pulse slicer of the input stage, the phase lead or lag between the input and output of ILRO occurs according to the input frequency. The proposed approach is digital-intensive enabling ultra-low power operation. The measured results show that the proposed demodulator can accurately demodulate GFSK signals with a simple structure. Furthermore, ultra-low power consumption and small active area of the architecture enables its use in many low power low cost wireless communication systems for IoT and MICS applications.

In the future, as the amount of phase differences according to 4-input frequencies can be accurately discriminated by using high-resolution time to digital converter, the proposed demodulator can be used in a QFSK demodulator.

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요 약 문

저전력 수신기 설계:
USN/IOT 용 주입 잠금 발진기를 이용한 다중 변조 모드 수신기

무선 수신기는 IoT 용 무선 센서 노드에서 가장 중요한 블록 중 하나입니다. 최근 전자산업 시장의 요구와 추세는 통신 장치가 더 낮은 전력 소비와 더 높은 성능을 요구합니다. 직접 변환 및 헤테로다인 방식과 같은 기존 수신기 구조는 성능이 높지만 저전력 동작은 매우 어렵습니다. 최근 발표되는 수신기는 간단한 구조의 장점을 갖는 OOK 변조를 사용하여 저전력의 동작을 구현했지만, 높은 수신 감도와 채널선택성을 달성하지 못했습니다. 이러한 단점을 해결하기 위해 본 논문에서 제안된 수신기의 핵심 구성 요소 인 주입 고정 LC 발진기를 사용한 저전력 수신기를 제안하였습니다. 또한 직접변환 방식 중 하나인 low-IF 수신기의 전력 소모를 줄이기 위해 주입 고정 링 발진기 기반의 저전력 복조기를 제안하였습니다.

본 논문에서는 제안된 수신기와 복조기의 핵심 블록 인 주입 고정 LC 및 링 발진기를 이론적으로 분석하여 주입 고정 현상을 더 잘 이해할 수 있도록 하였습니다. 주입 잠금 LC 발진기는 진폭, 주파수, 위상의 변화를 진폭으로 변환해 주는 특성을 가지며, 이러한 특성을 이용하면 OOK, BFSK, DPSK 와 같은 여러 변조 방식을 지원하는 수신기에 적용할 수 있습니다. 진폭 변조 신호를 사용하면 복조 및 하향 변환을 위해 간단한 포락선 검출기를 사용할 수 있습니다. 주입 잠금 링 발진기는 입력 주파수를 위상의 변화로 변환하는 특징을 가지고 있어 간단한 구조의 저전력 복조기에 사용이 가능합니다. 이러한 위상 변화를 하나의 D-플립플롭을 통해 식별이 가능하며, 이를 통해 최종적으로 수신된 데이터를 복원할 수있습니다.

본 논문의 주입 잠금 LC 발진기를 2.4GHz ISM 대역에서 동작하는 에너지 효율적인 다중 모드 수신기에 적용하였고, 이 수신기는 다양한 IoT 애플리케이션 시나리오에서 무선 센서 노드에 사용될 수 있습니다. 주입 잠금 LC 발진기는 수신기의 핵심 블록으로서, 주입 잠금 특성을 활용하여 OOK, BFSK 및 DBPSK 입력 신호의 진폭, 주파수 및 위상 변화를 각각 ILO 출력의 진폭 변동으로 변환합니다. 이 변환 과정 후에 간단한 포락선 검출을 수행하여 주입 잠금 LC 발진기의 출력 진폭 변화를 추출하고

신호를 기저 대역으로 하향 변환합니다. 결과적으로 믹서 및 주파수 합성기의 사용을 배제하여 전력 소비를 최소화 할 수 있습니다.

제안된 수신기는 이전의 주입 잠금 LC 발진기 기반 FSK 수신기와 달리 주입 잠금 LC 발진기의 입력 신호의 폐쇄 루프 제어를 구현한다는 것입니다. 제어 루프는 피크 검출기가 모니터링하는 기저 대역 신호 전력에 따라 SDA 의 이득을 조정합니다. 이 궤환을 통한 이득 제어가 없으면 수신기 입력 신호의 크기가 증가함에 따라 주입 잠금 LC 발진기 잠금 범위가 더 넓어지고 주파수 대 진폭 변환 성능이 저하되어 결국 복조 성능이 떨어집니다.

RF front-end 에서는 pre-amp 및 Q-enhanced SDA 를 사용하여 RF 입력 전력이 낮은 경우에도 충분히 큰 차동 주입 신호를 주입 잠금 LC 발진기에 제공하여 수신 감도를 크게 향상시킵니다. 또한 Q-Enhanced SDA 의 협대역 증폭 특성으로 인해 수신기의 채널선택성이 향상됩니다. 0.18μm CMOS 기술로 제작된 본 논문의 수신기는 1V 전원에서 324μW 를 소비하며, 50 kb/s 의 데이터 속도와 10^{-3} BER 에서 각각 OOK, BFSK 및 DBPSK 신호에 대해 –87, –85 및 –82dBm 의 감도를 달성하였습니다.

향후, 높은 integration level 을 위해 자동 이득 제어 루프를 IC 내부에 설계해야 합니다. 또한, 동작 전력을 더욱 줄이기 위해 제안된 수신기에 duty-cycle 조절 및 wake-up 수신기를 사용할 수 있습니다.

또한 본 논문에서는 low-IF 수신기 구조에 적합한 주입 잠금 링 발진기를 기반으로 한 새로운 GFSK 복조기를 제시하였습니다. low-IF 수신기 용 GFSK 복조기는 주입 잠금 링 발진기의 주파수-위상 변환 특성을 사용하여 설계 및 구현되었습니다. 입력 단의 pulse slicer 를 통해 신호의 펄스폭이 변화되고, 이 신호의 입력 주파수에 따라 주입 잠금 링 발진기의 입력과 출력 사이의 위상 리드 또는 지연이 발생합니다. 측정 결과 제안된 복조기는 간단한 구조로 GFSK 신호를 정확하게 복조 할 수 있음을 보여줍니다. 또한 초 저전력 소비와 복조기 회로의 작은 크기를 통해 IoT 및 MICS 애플리케이션을 위한 많은 저전력 저비용 무선 통신 시스템에서 사용할 수 있습니다. 향후 4 개의 입력 주파수에 따른 위상 변화량을 고해상도 시간-디지털 컨버터를 이용해 정확하게 판별한다면 제안된 복조기를 QFSK 신호 복원에 사용할 수 있습니다.

핵심어: 저전력 무선 수신기, 저전력 복조기, 주입 잠금 발진기, 포락선 검출