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## Effective mobility enhancement of amorphous In-Ga-Zn-O thin-film transistors by holographically generated periodic conductor

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In this study, we demonstrate a mobility enhancement structure for fully transparent amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) by embedding a holographically generated periodic nano-conductor in the back-channel regions. The intrinsic field-effect mobility was enhanced up to 2 times compared to that of a reference sample. The enhancement originated from a decrease in the effective channel length due to the highly conductive nano-conductor region. By combining conventional and holographic lithography, the performance of the a-IGZO TFT can be effectively improved without varying the composition of the channel layer. © 2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). [http://dx.doi.org/10.1063/1.4961379]

Amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) have attracted much attention due to their high field-effect mobility, high transparency, and good stability, which are mandatory requirements for high performance display applications. 1-3 The field-effect mobility value is a dominant parameter in determining the performance of such display devices. From a material viewpoint, indium is a key factor to determine the field-effect mobility in oxide-based TFTs. It has been reported that the molecular ratio among In, Ga, and Zn determines the performance of a-IGZO TFTs. Among the various molecular ratios, In:Ga:Zn=1:1:1 is widely chosen for a-IGZO active layers because the stable operation of an a-IGZO TFT can be guaranteed at this composition.<sup>4,5</sup> When In:Ga:Zn=1:1:1, the maximum field-effect mobility of the a-IGZO TFT that can be obtained from experiments is around 10 cm<sup>2</sup>/Vs. This must be further improved for high performance display applications. There have been tremendous efforts made to increase the field-effect mobility for transistors for the same channel layers. For typical silicon-based transistors, bridged-grain type polycrystalline silicon TFT has been developed by ion implantation of a conducting nano-structure in a channel region.<sup>6</sup> This method can be used to increase the field-effect mobility, but an additional ion implantation process is required to obtain a nano-conducting structure. For oxide-based TFTs, semiconductor/metal hybrid structures have been widely investigated. An indium-zinc-oxide/carbon nanotube hybrid structure, a-IGZO/silver nanowire arrays, and indium-tin-oxide (ITO)/aluminum9 have been applied to the channel region to increase the fieldeffect mobility. Another approach is to use simple plasma treatment to embed a nano-conductor in the channel region. It has been reported that embedding a nano hole structure in an a-IGZO TFT can enhance the field-effect mobility in the long channel length region. 10 Because it is not easy



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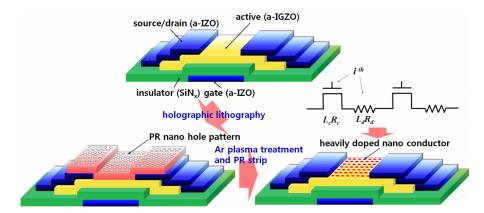


FIG. 1. Fabrication process of HTFT. Starting from conventional a-IGZO TFT, the HTFTs were fabricated using simple PR patterning by holographic lithography and Ar plasma treatment.

to vary the chemical composition in the channel region, the fabrication of nano-conductors via a simple plasma process is a more realistic method for next-generation TFT devices. For practical applications, it is necessary to scale down the channel length. For large area patterning of nano hole structures, holographic lithography is widely used in various areas, such as light-emitting diodes. <sup>11</sup> and photonic crystal devices. <sup>12</sup> Using holographic lithography, it is easy to fabricate periodic nano structures over large areas without additional fabrication processes.

In this paper, by introducing a holographically generated periodic nano-conductor in the back channel region (Holographic TFT;HTFT), we demonstrate an effective field-effect mobility enhancement structure using fully transparent a-IGZO TFTs; we analyze the electrical characteristics according to the channel length. The intrinsic electrical parameters between the HTFT and the reference TFT were systematically analyzed.

Figure 1 shows the a-IGZO TFTs (In:Ga:Zn=1:1:1 by mole fraction) with amorphous indiumzinc-oxide (In:Zn=9:1) gate/source/drain electrodes (G/S/D) fabricated on a glass substrate. We chose a-IZO for the G/S/D electrodes because it is one of the most widely used transparent electrodes. There has been prior work adopting IZO for the source/drain electrodes. 13 Compared to indium-tin-oxide (ITO) transparent electrodes, IZO electrodes show high transparency and good conductivity, especially when they are deposited at room temperature. No passivation layer was deposited for the post exposure process. The detailed fabrication process of the reference a-IGZO TFTs can be found elsewhere. 14 Next, a holographic lithography method was used to form photoresist (PR) nano hole patterns on the a-IGZO TFTs. The exposure was performed two times using negative PR. After the first exposure, a second exposure was performed after rotating the substrate 90°. Details of the patterning process have been reported elsewhere. 15 After development, a-IGZO TFTs having periodic PR nano hole patterns on the back channel region were prepared, as shown in Fig. 1. Figures 2(a) and 2(b) provide scanning electron microscopy images (SEM) of the PR nano hole periodic pattern after development. The period of the nano hole pattern was about 400 nm; the filling factor was in a range of 0.5 to 0.7, as shown in Figs. 2(a) and 2(b). Finally, Ar plasma treatment was performed on the fabricated a-IGZO TFTs having the PR nano hole patterns. It should be noted that the uncovered PR nano hole regions were exposed to Ar plasma and the conductivity of the nano hole regions increased due to an increase in the donor-like oxygen vacancies, 16 which formed a periodic nano-conductor in the back channel region.

Before electrical measurements, various material parameters of the active layer were analyzed. To confirm the amorphous phase of the a-IGZO active layer, X-ray diffraction (XRD) measurements were performed. Fig. 2(c) shows XRD data for the active layer before the plasma treatment. Two samples were prepared and annealed at 500 and 700 °C, which temperatures are higher than the process temperature used for the HTFT. It can be clearly seen that there is no sharp peak when the annealing temperature is 500 °C. The sharp peak at  $2\theta$ =31.08° can only be observed when the annealing temperature is 700 °C. Therefore, the IGZO active layers show amorphous phase under

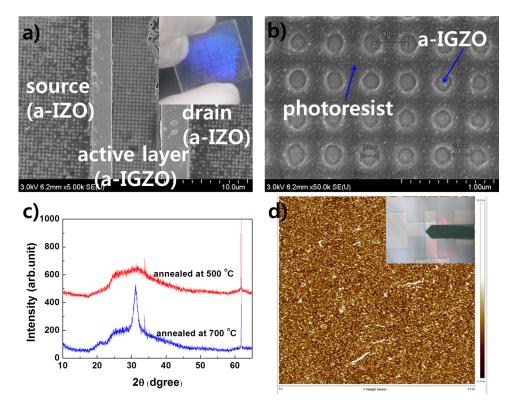


FIG. 2. (a) SEM image of PR patterned HTFT on a glass substrate. The inset shows a diffraction and interference color image produced by the PR nano hole pattern. (b) SEM image of PR patterns on the glass substrate. (c) XRD data of a-IGZO active layer before plasma treatment. (d) AFM image of HTFT in active region. Plasma treated and untreated regions could not be distinguished.

500 °C, indicating that the active layer of the HTFT is amorphous phase. These results are also consistent with prior work that showed a crystalline IGZO when the annealing temperature is over 700 °C. <sup>17</sup> Figure 2(d) shows an atomic force microscopy (AFM) image after nano conductors are formed in the back-channel region. Inset is a microscopy image in the channel region. The entire operation was carried out in tapping mode. The scan size was  $5 \times 5 \mu m$ . In the scan area, 12 periods of the nano-conductor are included. An amorphous phase of IGZO with small grain size was observed, which is consistent with the XRD data. The surface roughness ( $R_a$ ) was about 1.16 nm. It can be seen that no surface damage is induced by the plasma treatment because there is no difference in the plasma treated and untreated regions in the AFM image. It should be noted that the plasma power necessary to induce the oxygen vacancies is sufficiently weak to minimize the surface damage.

First, the electrical characteristics of the reference TFTs were measured. Then, the same samples were used to fabricate HTFTs. Accordingly, it is reasonable to assume that there was no sample-to-sample variation of the TFTs before or after the holographic lithography process. Figure 3(a) shows the transfer characteristics of the HTFTs and the reference TFTs. An increase in the drain current of the HTFT is observed when the channel length is long (L=100  $\mu$ m). In this case, the field-effect mobility of the HTFT increased about 1.8 times compared to that of the reference TFT. When the channel length is short (L=4  $\mu$ m), the drain current of the HTFT does not increase, as shown in Fig. 3(a), indicating that there is a channel length dependency of the field-effect mobility value of the HTFT, which may be due to parasitic resistance. To analyze the scaling effect of the HTFTs, field-effect mobility values were extracted as a function of channel length. Figure 3(b) shows the field-effect mobility values with respect to the channel length for the HTFTs and the reference TFTs. For long channel length HTFTs, significant increases of field-effect mobility of up to 3 times were observed when L > 10  $\mu$ m. It should be noted that the maximum

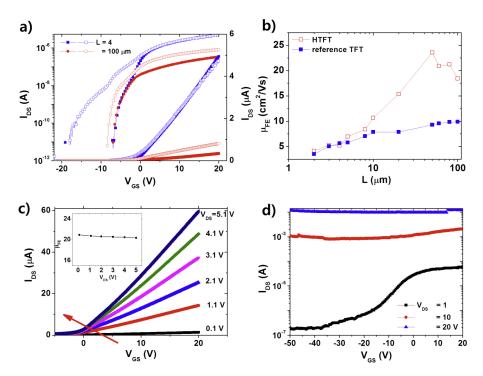


FIG. 3. (a) Transfer characteristics of reference (solid) and HTFT (open) for different channel lengths. ( $V_{DS}$ =0.1 V) (b) Scaling characteristics of field-effect mobility for reference (solid) and HTFT (open). The inset shows the transfer characteristics when L=60  $\mu$ m. (c) Transfer characteristics for  $V_{DS}$  ranging from 0.1 to 5.1 V when repeated measurements were performed. Inset is the field-effect mobility for different  $V_{DS}$  values. (d) Transfer characteristics of the a-IGZO TFT when the whole active region is exposed to Ar plasma.

field-effect mobility value of the HTFT was about 22.5 cm<sup>2</sup>/Vs, which is not easy to obtain without additional treatment processes. However, when the channel length is under 10  $\mu$ m, only a slight increase of the field-effect mobility is observed. This situation can be explained by simple modeling of the channel region. Because the electron density of the Ar plasma treated doping region (4.02 x  $10^{19}$ /cm<sup>3</sup> by Hall measurement) was much larger than that of the channel region ( $10^{18} \sim 10^{19}$ /cm<sup>3</sup>), the nano-conductor region can be modeled as a single resistor having a small resistance value which is independent of  $V_{GS}$ . Therefore, one period of a nano-conductor and a channel region can be modeled as a serial connection of a transistor and a resistor as shown in inset of Fig. 1. Theoretical analysis for the HTFT is similar with prior results of micro-size probing electrode structure. To calculate total resistance ( $R_{tot}$ ) in the active region along to a channel length direction, the following equation can be applied to the active region,

$$R_{tot} = R_{par} + \sum_{i}^{n} (L_c R_c + L_d R_d)_i \tag{1}$$

Here, n is the number of period,  $R_{par}$  is the parasitic resistance in the source/drain contact region,  $L_c$  and  $L_d$  are the length of  $i^{th}$  channel and nano-conductor region in one period,  $R_c$  and  $R_d$  are the resistance per unit length of  $i^{th}$  channel and nano-conductor region in one period, respectively. Because  $R_d$  is much smaller than  $R_c$ , total resistance in the active region can be simplified as,

$$R_{tot} \approx R'_{par} + nL_cR_c \tag{2}$$

Here,  $R'_{par}$  includes additional resistance of the nano-conductor region. If we assume the filling factor of the nano-conductor region as 0.5, the total resistance becomes,

$$R_{tot} \approx R'_{par} + \frac{LR_c}{2} \tag{3}$$

This indicates that the resistance of the active region decreases for the HTFT. In this case, because there is a parasitic resistance effect originated from the S/D contact region and the nano-conductor region ( $R'_{par}$  in eq. (3)), the increase of effective field-effect mobility is limited up to two times when  $R'_{par}$ =0.

Other electrical parameters such as threshold voltage  $(V_{TH})$ , subthreshold slope (SS), and defect density of states were extracted for the references and HTFTs. The interfacial trap density  $(D_{it})$  and bulk trap density  $(N_{bt})$  can be approximately calculated using the following equation, <sup>19</sup>

$$SS = \frac{k_B T}{q(\log e)} [1 + \frac{q^2}{C_{or}} (D_{it} + t N_{bt})]$$
 (4)

Where  $k_B$  is the Boltzmann constant,  $C_{ins}$  is the capacitance of the gate insulator per unit area, and t is the thickness of the active layer. It is reasonable to assume that  $D_{it}$  was not changed before and after Ar plasma treatment. Therefore, the difference of bulk trap density for the reference and HTFT is extracted using the following equation,

$$\Delta N_{bt} = \frac{C_{ox}}{tq^2} \frac{\Delta SS \log e}{k_B T/q} \tag{5}$$

Where  $\Delta SS$  is the difference of the subthreshold slope between the reference and HTFT. Extracted parameters were summarized in table I. For the HTFTs, negative shifts of  $V_{TH}$  and increases of SS and  $N_{bt}$  were observed. This is because donor-like oxygen vacancies ( $O_{vac}$ ) increase after Ar plasma treatment. It is known that the energy levels of the oxygen vacancies in the a-IGZO active layer are distributed in sub-bandgap region centered at 0.1 eV from the conduction band edge. The distribution of the energy level of  $O_{vac}$  is directly reflected to the subthreshold slope and threshold voltage. Because there is a trade-off between field-effect mobility and other parameters such as  $V_{TH}$  and SS, optimization of Ar plasma process is always necessary for the HTFT. In addition, relatively poor SS value and large  $\Delta N_{bt}$  of the short channel length HTFT is due to the effect of small open-area of Ar plasma process, which induces unexpected damage to target material. Further improvement of performance of short channel length HTFT can be archived when the end-point of plasma process is determined on the basis of the performance of the short channel length HTFT.

Concerning the stability of the HTFT, repeated measurements of the transfer characteristics were performed. Fig. 3(c) shows transfer characteristics for  $V_{DS}$  ranging from 0.1 to 5.1 V. Six times repeated measurements were applied for the same sample. There were slight negative shifts of threshold voltage ( $V_{TH}$ ) when  $V_{DS}$  increased from 0.1 to 5.1 V. These shifts may have been due to diffusion of oxygen vacancies from the plasma treated to untreated regions, originating from the lateral electric field in the channel region. However, the field-effect mobility did not change, as shown in inset of Fig. 3(c), indicating that the diffusion of oxygen vacancies did not degrade the performance of the HTFT.

Note that if the whole active region is exposed to Ar plasma, the active layer becomes conductive and the transfer curves show no on/off characteristics as shown in Fig. 3(d). This is consistent with prior experimental result when the electron density of the active layer is high.<sup>20</sup>

For a systematic analysis of the scaling characteristics of the HTFT and the reference TFT, the transmission line method (TLM) was applied, with results as shown in Figs. 4(a) and 4(b). For amorphous based TFTs with a bottom gate structure, starting from eq. (3), total resistance ( $R_{tot}$ ) can

TABLE I. A comparison of extracted parameters of  $V_{TH}$ , SS and  $\Delta N_{bt}$ .

Chanel length (TFT)	$V_{TH}\left( \mathrm{V}\right)$	SS (V/dec)	$\Delta N_{bt}$ (cm <sup>-2</sup> eV <sup>-1</sup> )
4 μm (reference)	-0.22	1.7	
4 μm (HTFT)	-0.80	4.4	$1.73 \times 10^{18}$
100 μm (reference)	-1.1	2.1	
100 μm (HTFT)	-3.0	2.4	$1.92 \times 10^{17}$

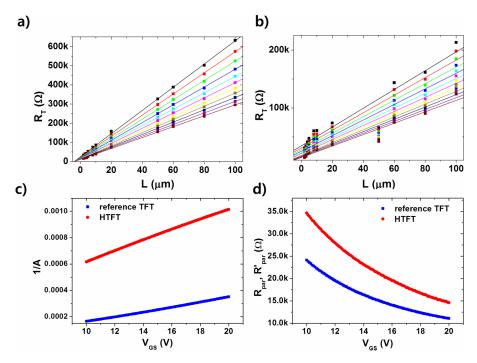


FIG. 4.  $R_T$  vs. L plots for (a) reference TFTs and (b) HTFTs. (c) Extraction of intrinsic field-effect mobility using Eq. (2). (d) Extracted parasitic resistance as a function of  $V_{GS}$  for reference TFT and HTFT.

be further resolved by the following equation.<sup>21</sup>

$$R_{tot} = L/[WC_{ins}\mu_{FEi}(V_{GS} - V_{Ti} - V_{DS}/2)] + R'_{par}$$
(6)

where W,  $\mu_{FEi}$ , and  $V_{Ti}$  are the channel width, the intrinsic field-effect mobility, and the intrinsic threshold voltage, respectively. From Eq. (6), the intrinsic field-effect mobility can be extracted using the following equation,

$$1/A = WC_{ins}\mu_{FEi}(V_{GS} - V_{Ti} - V_{DS}/2)$$
(7)

where A is the slope of  $R_{tot}$  vs. L. The slope of the curve shown in Fig. 4(c), corresponding to the coefficient of Eq. (7), denotes the intrinsic field-effect mobility. The resulting intrinsic field-effect mobility values extracted from Fig. 4(c) and Eq. (7) were about 10.9 cm<sup>2</sup>/Vs for the reference TFT and 21.8 cm<sup>2</sup>/Vs for the HTFT. The increase in intrinsic field-effect mobility originates from the periodic nano-conductor region. The HTFT comprises series connections of the nano-conductor and the channel regions along the channel length direction. Therefore, the physical channel length decreased due to the highly conductive nano-conductor region, which induces a decrease in the effective channel length. <sup>18</sup>

Meanwhile, after Ar plasma exposure, overall parasitic resistance increased. Fig. 4(d) shows the parasitic resistance for the HTFT and for the reference TFT. It can be seen that the parasitic resistance of the HTFT increased up to 1.4 times after Ar plasma exposure. The increase of the parasitic resistance induced a channel length dependent scaling effect, as shown in Fig. 3(b). It has previously been found that Ar plasma treatment increases the conductivity, but only near the surface of the a-IGZO layer. <sup>12</sup> In this case, the new current path from the channel region to the highly conductive back surface region can be one origin of the increase of parasitic resistance.

To further analyze the current flow in the active layer of the HTFT, TCAD simulation (from Silvaco Inc.) was performed. Conventional material parameters for the a-IGZO active layer and the SiNx gate insulator were used. Figure 5(a) shows the HTFT device structure for the simulation; this structure has a nano-conductor region in the back channel. The channel length was 4  $\mu$ m and the channel width was 60  $\mu$ m. The thickness of the active layer was 80 nm. The doping density and the period of the nano-conductor regions were set to  $2 \times 10^{19}$  cm<sup>-3</sup> and 400 nm, respectively.

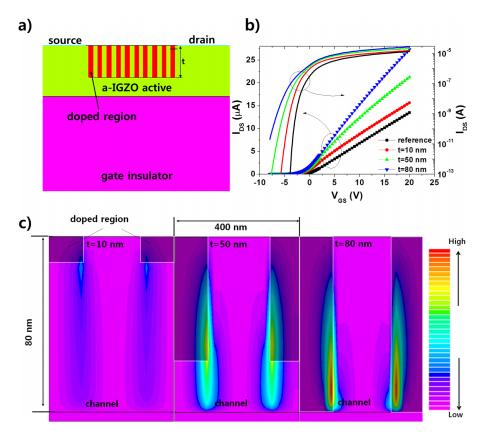


FIG. 5. (a) Cross-sectional view of the HTFT structure for the simulation. 't' is the thickness of the doped region. (b) Simulation results for the transfer characteristics of the HTFT for different  $t(V_{DS}=0.1 \text{ V})$ . (c) Vertical component of the current density of the HTFT in one period.

The simulation was performed by varying the thickness of the doped regions (t) from 10 to 80 nm. Figure 5(b) shows transfer the characteristics of the HTFT for different values of t. Compared to that of the reference TFT, the drain current of the HTFT increased up to 2.2 times when the nano-conductor regions covered the whole active region (t=80 nm). Similar with experimental results, there were also negative shifts of  $V_{TH}$  and increases of SS when the nano-conductor region exists. When the nano-conductor region only partially covered the active region (t=10 and 50 nm), however, the increase of the drain current was relatively small. In addition, roll-over of the transfer curve was also observed when t=10 and 50 nm. Figure 5(c) shows the vertical component of the current density for one period of the doped region. When t is increased, the vertical component of the current density and the total drain current increased concurrently, as shown in Figs. 5(b) and 5(c). The magnitude of vertical component of current density determines whether the resistance of nano-conductor region is negligible because when the thickness of nano-conductor region increased, current spreading through the nano-conductor region also increased. In example, if the thickness of the nano-conductor region is 10 nm, vertical component of current density is small and most of electron flows through the lateral channel direction as if there is no nano-conductor region. In this case, the HTFT works similar with conventional TFT. However, if the nano-conductor region covers whole active layer (t=80 nm), the current spreading through nano-conductor region increases and the region can be considered as low resistance conducting area which is modeled as eq. (2). Therefore, the effective field-effect mobility increased only when the nano-conductor region is thick and resistance of nano-conductor region is sufficiently low.

Because the nano-conductor region in the back channel creates a highly conductive current path, the increase of the field-effect mobility of the HTFT originates from the decrease of the effective channel length. When the nano-conductor region is partially doped, the undoped area

of the region reduces the effect of new conductive current path in the back channel and become a bottle-neck against HTFT performance improvement. There is an alternative method that can be used to replace the Ar plasma treatment. It is known that  $H_2$  plasma treatment can dope  $H_2$  molecules deeply into the active layer.<sup>23</sup> Hydrogen doped zinc-oxide film can be used to replace the typical indium-tin-oxide film because sheet resistance can be lowered under  $200 \ \Omega/\Box$ .<sup>24</sup> Therefore, it is expected that the increase of the parasitic resistance can be further reduced using  $H_2$  plasma treatment instead of Ar plasma treatment.

In conclusion, we have demonstrated a-IGZO TFTs embedded with holographically patterned conductive nano hole regions. After holographic lithography and Ar plasma treatment, the intrinsic field-effect mobility of the HTFT increased up to 2 times in comparison with that of the reference TFTs. The improvement mechanism of the field-effect mobility of the HTFT was analyzed by TCAD simulation, and we found that the new current path in the back channel is the origin of the increase of the effective field-effect mobility of the HTFT. Therefore, the performance of a-IGZO TFTs can be further improved without significant effort, simply by using the combination of conventional and holographic lithography.

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