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Gate voltage and drain current stress instabilities in amorphous In–Ga–Zn–O thin-film transistors with an asymmetric graphene electrode

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The gate voltage and drain current stress instabilities in amorphous In–Ga–Zn–O thin-film transistors (a-IGZO TFTs) having an asymmetric graphene electrode structure are studied. A large positive shift in the threshold voltage, which is well fitted to a stretched-exponential equation, and an increase in the subthreshold slope are observed when drain current stress is applied. This is due to an increase in temperature caused by power dissipation in the graphene/a-IGZO contact region, in addition to the channel region, which is different from the behavior in a-IGZO TFTs with a conventional transparent electrode. © *2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.* [http://dx.doi.org/10.1063/1.4931084]

I. INTRODUCTION

Carbon single-layer graphene and amorphous indium-gallium-zinc-oxide (a-IGZO) semiconductors are considered to be representative next-generation transparent electrodes and high-performance semiconductors, respectively.[1–6] Their combination is expected to enable new opportunities in emerging display device applications such as curved or flexible transparent electronic devices.[7,8] In particular, graphene is expected to replace conventional transparent oxide-based conductive electrodes such as indium tin oxide (ITO)[9] and indium zinc oxide (IZO)[10] because of the increasing demand for indium free transparent electrodes. However, sufficient progress has not been made in the application of graphene electrodes to a-IGZO TFTs owing to a lack of understanding of the underlying physics between graphene and the semiconductor layers. We recently reported the electrical characteristics of a-IGZO TFTs with an asymmetric graphene electrode and a probe electrode on the drain side.[11] We found that the a-IGZO active layer and graphene electrode form a Schottky contact, and the electrical characteristics exhibit a polarity depending on the direction of the drain voltage due to the Schottky barrier effect and the high parasitic resistance under the graphene electrode in the a-IGZO active layer. One of the important issues regarding a-IGZO TFTs with graphene electrode is the gate voltage and drain current stress instability behaviors, which is related to Schottky contact between the a-IGZO semiconductor and the graphene electrode. Nevertheless, a-IGZO TFTs with a graphene electrode have not been adequately studied.

Here, we investigated the gate voltage and drain current stress instabilities of a-IGZO TFTs with an asymmetric graphene electrode. An asymmetric graphene electrode structure was adopted to characterize the drain current stress effect of pure graphene on the a-IGZO TFTs because a high current level cannot be obtained when a graphene electrode is used on both sides of the

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source/drain (S/D) electrodes without an additional doping process in the contact region. We found that the polarity of the applied drain to source voltage (V_{DS}) plays a crucial role in the drain current stress instability of a-IGZO TFTs with asymmetric graphene S/D electrodes, and that this is closely related to Joule heating and an increase in electron trapping into the insulator.

II. EXPERIMENTAL DETAILS

Graphene sheets were synthesized on a Cu foil (Sigma Aldrich) by thermal chemical vapor deposition (CVD). The quality of the CVD grown graphene was monitored by Raman spectroscopy and optical microscopy [inset of Figure 1(a)]. Monolayer graphene was well synthesized, as confirmed by the I_{2D}/I_G ratio. The sheet resistance of graphene was approximately 238 $\Omega/\square$ @5 V according to a two-point measurement. The prepared graphene sheet was transferred to fabricated a-IGZO TFTs with conventional a-IZO S/D electrodes. Then, the graphene electrode was patterned by conventional photolithography and a reactive ion etching process using oxygen plasma. Accordingly, the graphene quality is not changed before and after the patterning process. The detailed
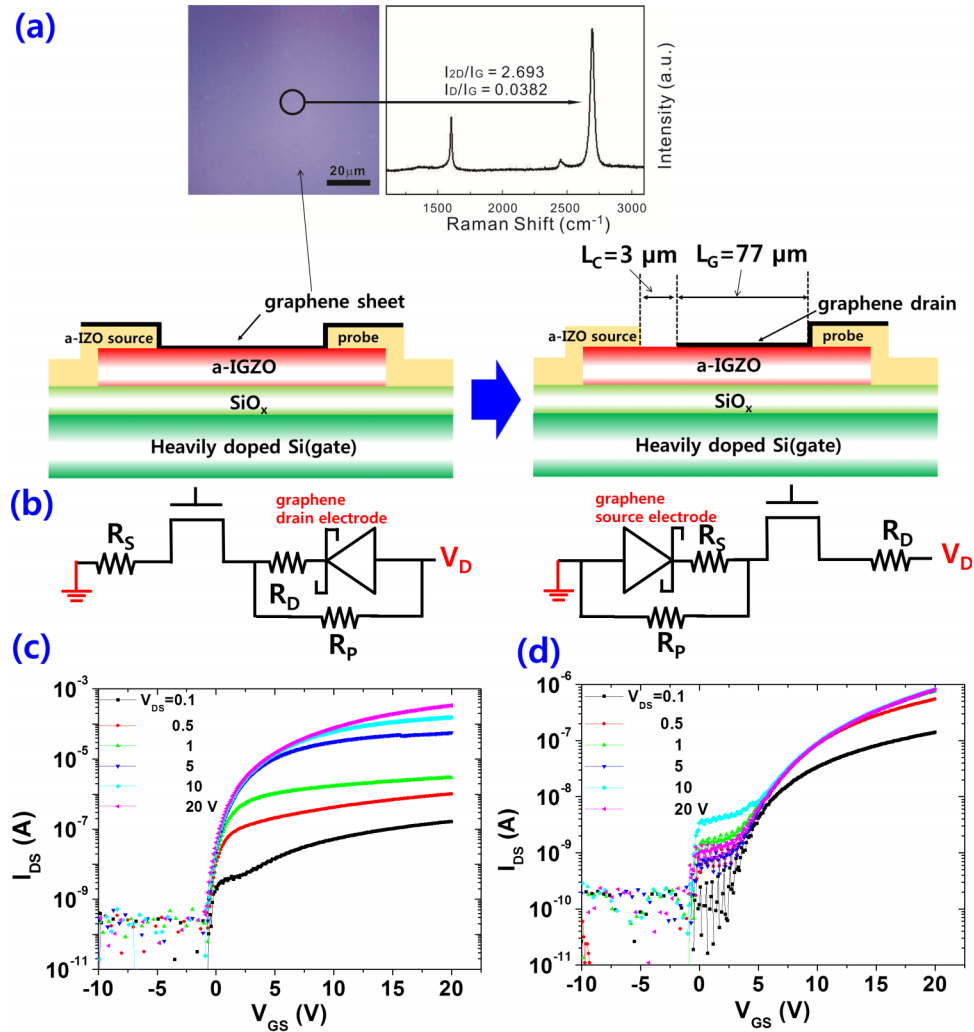

FIG. 1. (a) Patterning of an asymmetric graphene electrode structure. An optical micrograph and a Raman spectrum are shown in the upper left, which confirm a single layer of graphene. (b) Equivalent-circuit models for the graphene drain (left) and graphene source (right) connections. The current flow into the probe electrode is negligible owing to the high resistance of the active region (R_P) under the graphene electrode for both cases. Transfer characteristics of an a-IGZO TFT with an asymmetric graphene electrode using (c) GrD and (d) GrS connections.

fabrication process for the graphene sheet and the a-IGZO TFTs with a-IZO S/D electrodes can be found elsewhere.[11,12] Graphene was patterned to form an asymmetric drain structure, as shown in Figure 1(a). Graphene and a-IZO form a dual electrode structure, especially when graphene/a-IZO is connected on the drain side. The structure is useful for directly comparing the variation in the electrical characteristics before and after transferring the graphene electrode. In addition, the a-IZO electrode on the drain side acts as a probe electrode to detect the electrical characteristics under the graphene electrode as a function of the applied voltage. The channel length (L_C) was about 3 μm, the channel width (W) was about 60 μm, and the distance from a channel edge to the a-IZO probe L_G was about 77 μm, as shown in Figure 1(a). The threshold voltage was defined as the value of the gate to source voltage (V_{GS}) when the drain current $I_{DS} = 10^{-7}$ A. The field-effect mobility in the saturation region ($V_{DS} = 20$ V) was 5.6 cm^2/Vs when the channel length was defined as L_C shown in Figure 1(a).

III. BIAS AND CURRENT STRESS INSTABILITY OF a-IGZO TFTs WITH CONVENTIONAL a-IZO S/D ELECTRODES

Figures 1(c) and 1(d) show the transfer characteristics of a-IGZO TFTs with an asymmetric graphene electrode structure when the graphene electrode is connected on the drain side (GrD connection) and source side (GrS connection), respectively. The I_{DS} level exhibits rectifying and blocking characteristics for the GrD and GrS connections, respectively. In particular, the I_{DS} level was considerably decreased for the GrS connection owing to the blocking state between graphene and the a-IGZO active layer, inducing a depletion region and high parasitic resistance from the bulk region under the drain electrode. In this case, the current flow from the drain electrode to the source electrode is very low, even though there is an additional probe electrode on the source side, which is consistent with a previous result.[11] For the GrD connection, the amount of current flow from the source to the probe electrode can be negligible because L_C is much smaller than L_G. Therefore, we can confirm that graphene acts as a real electrode, and the probe electrode structure can be used to compare the electrical characteristics before and after transferring the graphene electrode without disturbing the current voltage characteristics of the TFTs.[11] The equivalent circuits for the GrD and GrS connections are modeled as shown in Figure 1(b).

First, gate voltage ($V_{GS} = 20$ V and $V_{DS} = 0$ V) and drain current ($V_{GS} = 20$ V and $V_{DS} = 20$ V) stress instabilities were consecutively measured for 3600 s for a-IGZO TFTs with conventional a-IZO electrodes on both sides of the source and drain electrodes. In order to measure the effect of the drain current stress more clearly, we used a short channel length TFT (the channel length was about 2 μm and the channel width was about 100 μm). Because the S/D electrodes have a symmetric structure, the stress tests were performed by applying V_{GS} and V_{DS} through a single direction. The transfer characteristics were measured every 100 s.

Figures 2(a) and 2(b) show the evolution of the transfer characteristics for the gate voltage and drain current stress conditions, respectively. Main panels and insets are forward and reverse sweep results, respectively. Positive shifts in the threshold voltage were observed for the gate voltage and drain current stress conditions. However, the magnitude of the threshold voltage shift and the variation in the subthreshold slope respectively differ depending on the gate voltage and drain current stress conditions. The threshold voltage was shifted more in the positive direction, and the transfer curve exhibited hump-like behavior in the subthreshold voltage region for the drain current stress conditions. It is known that a high gate voltage stress induces hump-like characteristics with a negative shift in the transfer curve in the subthreshold voltage region for a-IGZO TFTs owing to the formation of a parasitic transistor[13] or hole trapping in the back-channel region.[14] However, in the present case, the hump-like transfer curve shifted in the positive direction for the drain current stress conditions, and the transfer curve exhibited no recovery behavior under drain current stress conditions, as shown in Figure 2(b). It was recently reported that migration of positively charged mobile Zn interstitials accumulated at the back channel region can be an origin of hump-like characteristics under a positive bias stress condition.[15] In the present case, because we used a-IZO as the S/D electrodes, current stress can enhance the migration of Zn ions and prominent hump-like characteristics are observed for the drain stress condition, as shown in Figure 2(b). It should be noted
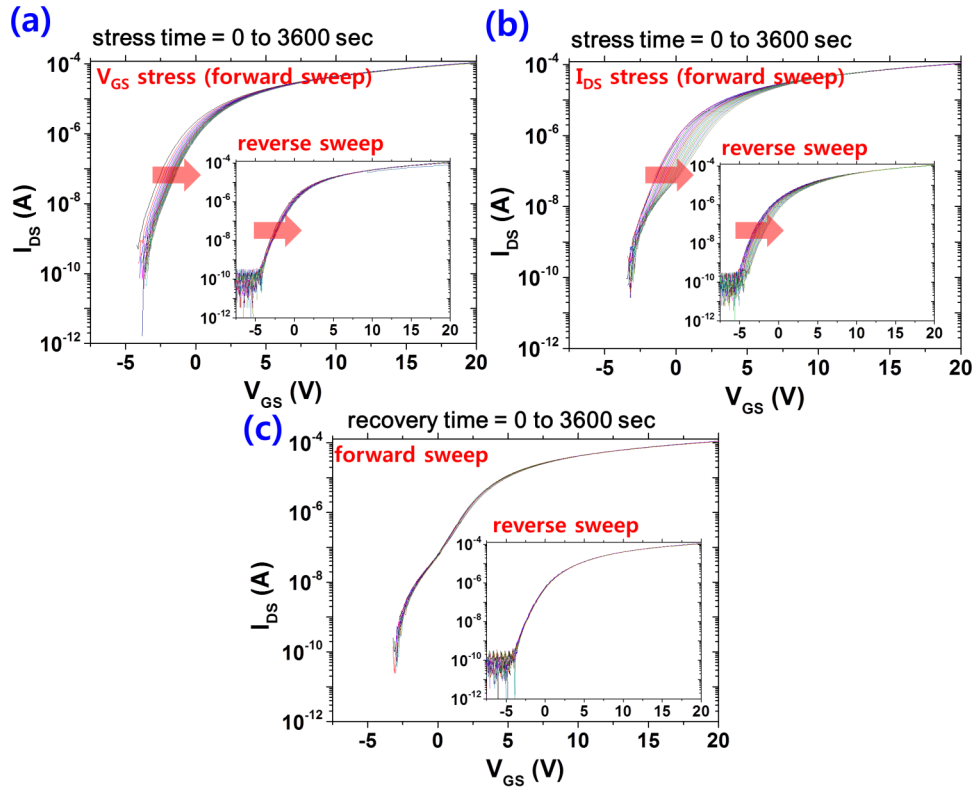
FIG. 2. Evolution of the transfer characteristics of an a-IGZO TFT with conventional a-IZO S/D transparent electrodes under (a) a gate voltage stress ($V_{GS} = 20$ V, $V_{DS} = 0$ V) and (b) a drain current stress ($V_{GS} = 20$ V, $V_{DS} = 20$ V). Each measurement was performed at $V_{DS} = 1$ V. (c) Recovery behavior of the transfer characteristics for 3600 s after stress is removed. The insets of (a), (b), and (c) show the evolution of transfer characteristics under a reverse sweep.

that the hump-like characteristics are observed only for the forward sweep condition. This indicates that the variation of the electrical characteristics in the channel region is asymmetric, and the defect formation region is highly localized near the drain side contact region. Figure 2(c) and the inset of Figure 2(c) show the recovery behaviors of transfer characteristics after the drain current stress is removed. Recovery behavior was not observed for either forward or reverse sweep conditions.

IV. BIAS AND CURRENT STRESS INSTABILITY OF a-IGZO TFTs WITH GRAPHENE ELECTRODE

Next, the gate voltage and drain current stress instabilities were measured for the a-IGZO TFT with the asymmetric graphene electrode. First, the gate voltage stress instability ($V_{GS} = 20$ V and $V_{DS} = 0$ V) was measured with the GrD connection, and the same measurement was performed with the GrS connection. The drain current stress instability ($V_{GS} = 20$ V and $V_{DS} = 20$ V) was also measured using the same TFT for the GrD and GrS connections, consecutively.

Figure 2(a) and the inset of Figure 2(a) show the evolution of the transfer characteristics for the a-IGZO TFT for $V_{GS} = 20$ V and $V_{DS} = 0$ V with the GrD and GrS connections, respectively. It is observed that prolonged gate voltage stress induced a slight positive shift in the threshold voltage after 3600 s for both the GrD and GrS connections. Although the initial ON current level and subthreshold slope of the TFT strongly depend on the polarity of the connection, the gate voltage stress instability was independent of the polarity of the V_{DS} connection. This is because charge trapping, which depends on an electric field along the vertical direction, is the dominant factor for the gate voltage stress instability. In this case, there are no variations in the subthreshold slope and field-effect mobility according to the stress time.
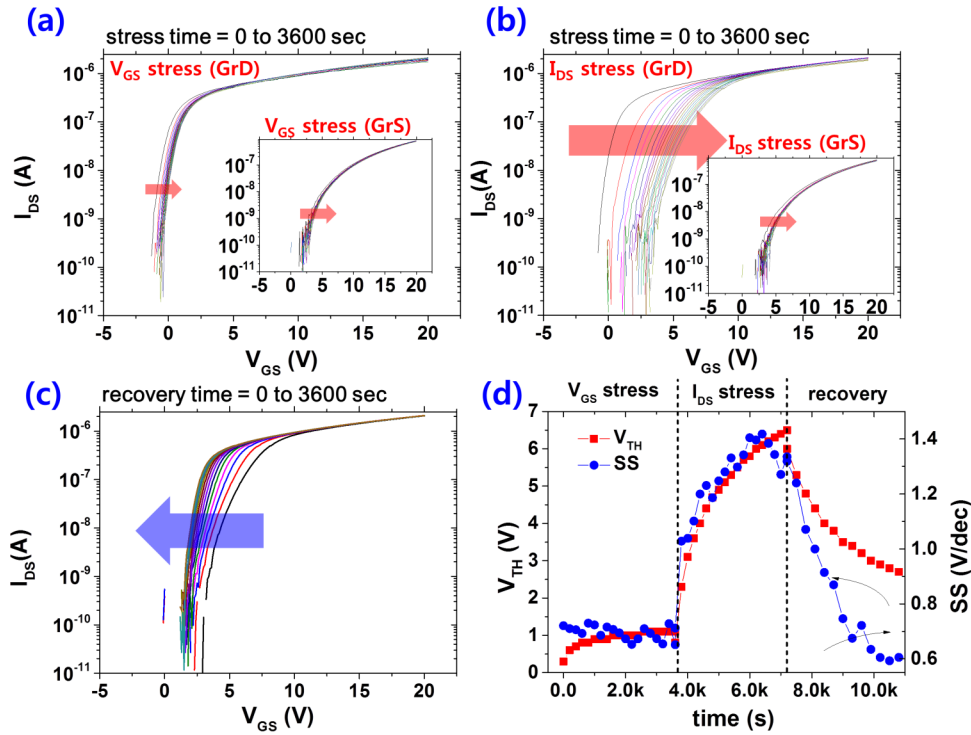
FIG. 3. Evolution of the transfer characteristics of an a-IGZO TFT with an asymmetric graphene electrode under (a) a gate voltage stress (V_{GS} = 20 V, V_{DS} = 0 V) and (b) a drain current stress (V_{GS} = 20 V, V_{DS} = 20 V). The main panels and insets are the results from GrD and GrS connections, respectively. (c) Recovery behavior of the transfer characteristics for 3600 s. (d) Evolution of the threshold voltage and subthreshold slope for the gate voltage and drain current stresses as well as the recovery conditions. All transfer characteristics were measured at V_{DS} = 1 V.

However, the evolution of the transfer characteristics critically depends on the polarity when a drain voltage or drain current stress is applied. Figure 3(b) and the inset of Figure 3(b) show the evolution of the transfer characteristics for the a-IGZO TFT for V_{GS} = 20 V and V_{DS} = 20 V with GrD and GrS connections, respectively. There is a large threshold voltage shift in the positive direction as well as a significant increase in the subthreshold slope for the GrD connection, as shown in Figsures 3(b) and 3(d). The threshold voltage shifted up to approximately 6 V, and the subthreshold slope increased by more than two times, which is typically observed when high current stress is applied,[16] associated with charge trapping in shallow trap sites of the a-IGZO/insulator interface. The variation in the subthreshold slope and the threshold voltage shift were nearly recovered after 3600 s, as shown in Figures 3(c) and 3(d). On the other hand, there is only a slight positive shift in the threshold voltage for the GrS connection, consistent with the result for the gate voltage stress instability in Fig 3(a). Therefore, the drain current stress (not the drain voltage stress) is the main origin of the variations in the threshold voltage and subthreshold slope.

There are two possible explanations for the large threshold voltage shift and the decrease in the subthreshold slope for the GrD connection. First, new acceptor-like defect states that diffuse from the graphene electrode could be generated under drain voltage stress conditions. It was reported that carbon functions as an acceptor-like defect state, forming carbon–oxygen complex defects when annealed in an oxygen-poor atmosphere.[17] However, the subthreshold slope recovered to its initial state, which is not possible when diffused carbon is the source of acceptor-like defect states. In addition, the graphene electrode would be stable at the temperature of the drain current stress conditions because graphene was synthesized at a very high temperature (~1000 °C). Second, the drain current stress generates heat dissipation, which causes a local thermal effect in the active layer, resulting in an increase in the temperature and electron trapping ratio to the gate insulator.[18,19] This effect is accelerated as the temperature increases and exhibits recovery behavior, which is consistent with our case. This also can be confirmed by modeling of the threshold voltage shift (ΔV_{TH}) as
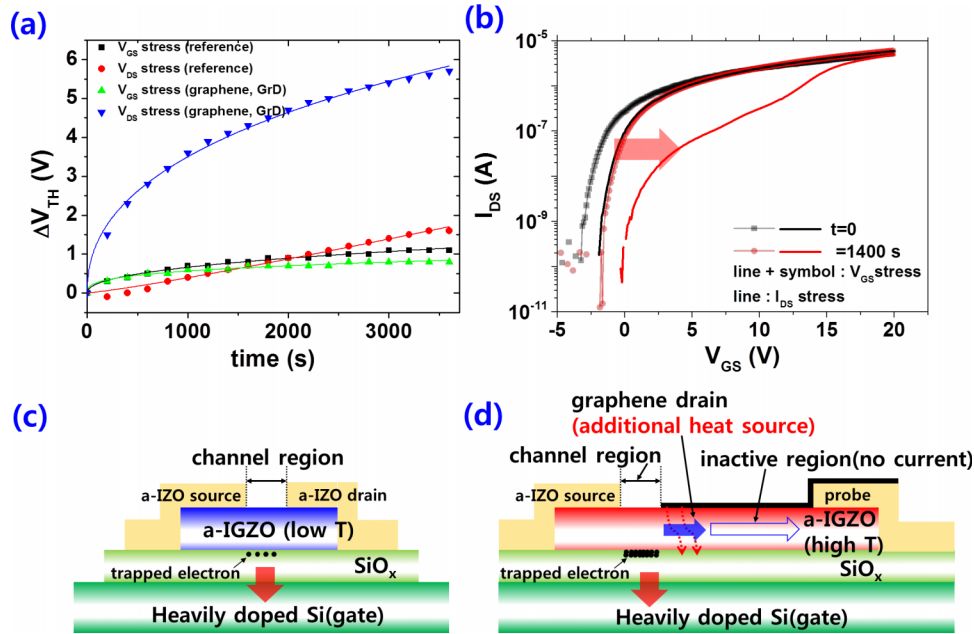
FIG. 4. (a) ΔV_{TH} *vs.* stress time for different conditions (measurement: symbol, stretched-exponential fitting: line). (b) Evolution of transfer characteristics of an a-IGZO TFT with small L_G ($L_G = 17$ μm) and the same channel length ($L_C = 3$ μm) under successive gate voltage ($V_{GS} = 20$ V, $V_{DS} = 0$ V) and drain current stress conditions ($V_{GS} = 20$ V, $V_{DS} = 10$ V). Heat generation and flow under drain current stress conditions: (c) a-IGZO TFT with a-IZO S/D electrodes and (d) a-IGZO TFT with an asymmetric graphene electrode. More electrons are trapped near the gate insulator when the graphene/IGZO contact region acts as an additional heat source.

a function of stress time, as shown in Figure 4(a). It is known that ΔV_{TH} can be modeled as a stretched-exponential equation when charge trapping is the dominant mechanism for the instability of TFTs, which is given as,[20–22]

$$\Delta V_{TH} = V_{TH0}(1 - \exp(-(t/\tau)^{\beta})) \qquad (1)$$

Here, V_{TH0} is the saturation voltage, τ is the characteristic time, and β is the stretched-exponential exponent. The ΔV_{TH} *vs.* time graph fitted the stretched exponential equation well, as shown in Figure 4(a). For the TFT with the graphene electrode (GrD connection), the fitted τ and β values were about 6.7×10^7 s and 0.32 for gate voltage stress and 3.3×10^4 s and 0.46 for drain current stress, respectively. For the reference TFT, the fitted τ and β values were about 2.7×10^6 s and 0.44 for gate voltage stress and 3.0×10^4 s and 1.2 for drain current stress, respectively. A tremendous decrease in τ of up to two orders of magnitude was observed when drain current stress was applied to the TFT with the graphene electrode, indicating that the barriers of trap sites are lowered due to the increase in temperature by power dissipation. It should be noted that the β value was very large for the reference TFT under drain current stress, revealing that the governing mechanism is different from the other cases and is not charge trapping, as mentioned before. Therefore, based on recovery behavior and the modeling of ΔV_{TH}, we can confirm that the origin of the instability of the TFTs with the graphene electrode under drain current stress is the increase in temperature.

By comparing the results from the a-IGZO TFTs with the a-IZO electrodes in Figure 2(b), the thermal effect did not solely originate from power dissipation in the channel region, which can be confirmed from the different recovery behaviors in Figure 3(c) and the inset of Figure 2(b). In addition to the channel region, graphene or (and) a graphene/a-IGZO contact region on the drain side can be a heat source, and causes an increase in the temperature and charge trapping ratio in the gate insulator. Graphene possesses a large sheet resistance (~238 Ω/□) compared to conventional a-IZO electrodes (~50 Ω/□), leading to power dissipation in the graphene electrode, especially when drain current stress is applied. It was also reported that a graphene sheet can be used as a transparent heater when the sheet resistance is sufficiently high.[23] The dominant origin of the large performance

variation can be verified through comparison with a TFT having a small L_G and a poor contact property corresponding to a small field-effect mobility value. The gate voltage and drain current stress instability were measured for a TFT with small L_G (L_G = 17 μm) and poor contact property (field-effect mobility in the saturation region = 3.0cm^2/Vs) for 1400 s, consecutively, as shown in Figure 4(b). In this case, it is expected that ΔV_{TH} will be small if the resistance of the graphene electrode is dominant for power dissipation. However, there is a large ΔV_{TH} shift with a deterioration of the subthreshold slope under the drain current stress condition. Even when we applied small drain voltage (V_{GS} = 20 V, V_{DS} = 10 V) and small stress time for drain current stress, the increase in V_{TH} and the subthreshold slope was larger than that of the TFT with large L_G. This reveals that the graphene/a-IGZO contact property of each device determines the power dissipation dominantly, which is independent of L_G because the current spreading length is typically smaller than several micrometers from the edge of S/D electrodes, as shown in Figure 4(d), and much smaller than L_G.[24] This explains the L_G independent ΔV_{TH} of the TFTs under the drain current stress condition. In addition, there are many defect sites in graphene,[25] which can influence on contact property and induce Fermi level pinning. Even for a large V_{DS}, the Schottky contact induces a voltage drop in the contact region, leading to power dissipation and Joule heating, as shown in Figures 4(c) and 4(d). We can therefore conclude that the contact property is the dominant factor responsible for power dissipation in the a-IGZO/graphene structure. The unexpected thermal effect of the graphene electrode can further increase when a glass substrate is used owing to its low thermal conductivity. Controlling the heat dissipation thus plays an important role in the drain current stress instability of the a-IGZO TFT with a graphene electrode, particularly when a high current stress is applied. This should be overcome in order to improve the stability of a-IGZO TFTs with graphene electrodes.

V. CONCLUSION

In conclusion, gate voltage and drain current stress instabilities of a-IGZO TFTs with an asymmetric graphene electrode structure were analyzed. An unexpected thermal effect induced instabilities in the a-IGZO TFTs with a graphene electrode under drain current stress conditions owing to power dissipation in the graphene/a-IGZO contact region. This further increases the threshold voltage shift and subthreshold slope in comparison with the values obtained under voltage stress conditions. It is known that a graphene sheet fabricated by CVD exhibits a relatively large number of defects compared to conventional transparent electrodes and the contact property between the graphene and the a-IGZO active layer critically depends on the quality of the graphene electrode. Fabrication of defect free and high quality graphene is therefore essential for further improvement in the stability of a-IGZO TFTs with graphene electrodes.

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