Master's Thesis

석사 학위논문

Low-Power Analog Baseband Circuits for Wake-Up Receivers

Seungyeob Baik (백 승 엽 白 承 燁)

Department of Information and Communication Engineering

정보통신융합공학전공

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Advisor: Professor Junghyup Lee

Co-Advisor: Professor Minkyu Je

By

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Department of Information and Communication Engineering

DGIST

A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Master of Science in the Department of Information and Communication Engineering. The study was conducted in accordance with Code of Research Ethics[1)].

Nov. 25. 2016

Approved by

Professor Junghyup Lee (Signature)

(Advisor)

Professor Minkyu Je (Signature)

(Co-Advisor)

1) Declaration of Ethical Conduct in Research**:** I, as a graduate student of DGIST, hereby declare that I have not committed any acts that may damage the credibility of my research. These include, but are not limited to: falsification, thesis written by someone else, distortion of research findings or plagiarism. I affirm that my thesis contains honest conclusions based on my own careful research under the guidance of my thesis advisor.

Low-Power Analog Baseband Circuits for Wake-Up Receivers

Seungyeob Baik

Accepted in partial fulfillment of the requirements for the degree of
Master of Science

Nov. 25. 2016

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Abstract

Wireless sensor networks require ultra-low power consumption. To avoid wasting power consumption, wake up receiver system is applied to main receiver system. The wake up receiver continuously watch a wake up signal from other nodes. If it detects a wake up signal, it activates the main receiver to receive data.

The baseband circuit for wake up receiver is composed of envelope detector, programmable gain amplifier and comparator. The enveloped detector converts the high frequency signal to baseband signal. The output signal of envelope detector is amplified through the programmable gain amplifier suitably. The comparator determines that the output signal of the programmable gain amplifier is high or low.

This baseband circuit uses fully differential structure to strong from environment noise and coupling noise. The gain of programmable gain amplifier is defined by the ratio of capacitor value through negative feedback network. Moreover, the comparator not only consume power only when the input signal cross the threshold voltage, but also apply a replica biasing circuit with negative feedback to achieve low power consumption and be strong from PVT variation. This system is designed in 180nm technology and the total current consumption is under 14μA, when the supply voltage is 1.8V.

Keywords: Wake up receiver, Baseband, Envelope detector, Programmable gain amplifier, Comparator

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I. Introduction

The wireless sensor network is a large network of wireless connected nodes. Nowadays internet of things is used everywhere. Internet of things means that all stuffs are connected each other and exchange their information when they need. For example, if someone want to check how much electricity he uses every day, just put a read sensor and the sensor transmit information to control center every day. He doesn't need to read the number by himself. Another example is a smart home system. We can control all of things like television, air conditioner, washing machine and so on by using cell phone.

However, there are some issue when we design transceiver and receiver which are in the module for getting and transmitting information. First, power consumption is the biggest problem that we have to solve [1]. It is also battery issue. Network is large with many nodes. So battery charge or replacement is not easy, expensive, or even impossible. Engineer has to design that the node works more than 10 years, without running out of power. Second problem is the size. All sensor node need to be small to insult in the module. It also relates with the cost. For circuit engineer, chip area is the cost. Even though CMOS technology is developed, resistor, capacitor and inductor are still large comparing NMOS and PMOS. Many engineer have been researching to make chip as small as possible.

Those things what I mentioned are interacting each other. For example, battery is going to small as the size is small. So the node cannot accompany large battery to use for a long time. For this reason, reducing power consumption of the node is the effective way to minimize the size. Few years ago, the VDD was around 5V, but now 1.8V or 1.2V is common. It is also hard for circuit engineer to design circuit, because the short channel process has much noise than

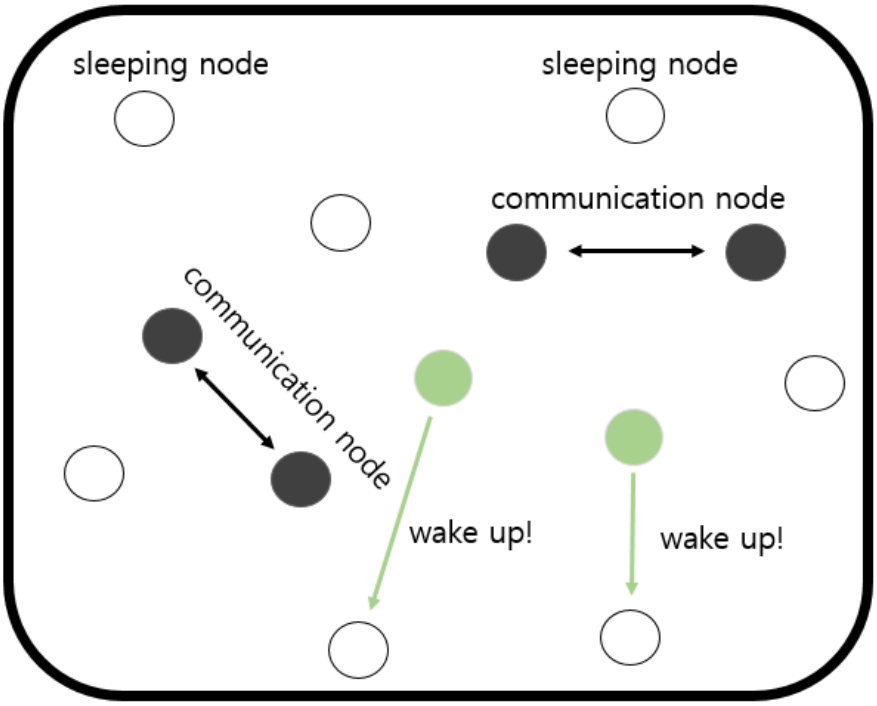

Figure 1.1. Wireless sensor network environment

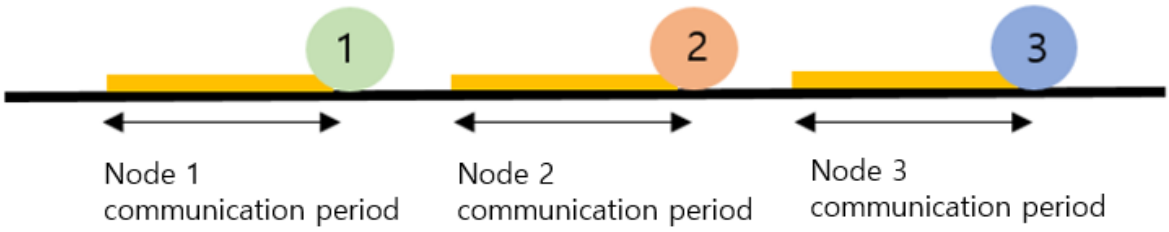

Figure 1.2. Duty cycling system of wireless sensor network

the long channel process. Noise is important factor for designing circuit. I will explain about the noise at chapter III.

Obviously, reducing power consumption is a key method to accomplish the goals of the wireless sensor network. There are two popular methods to minimize power consumption. First, duty-cycling is a very useful way to reduce energy usage and boost battery life [2]. The node is turned on for short period of time to operate function and then gone to low power mode. The

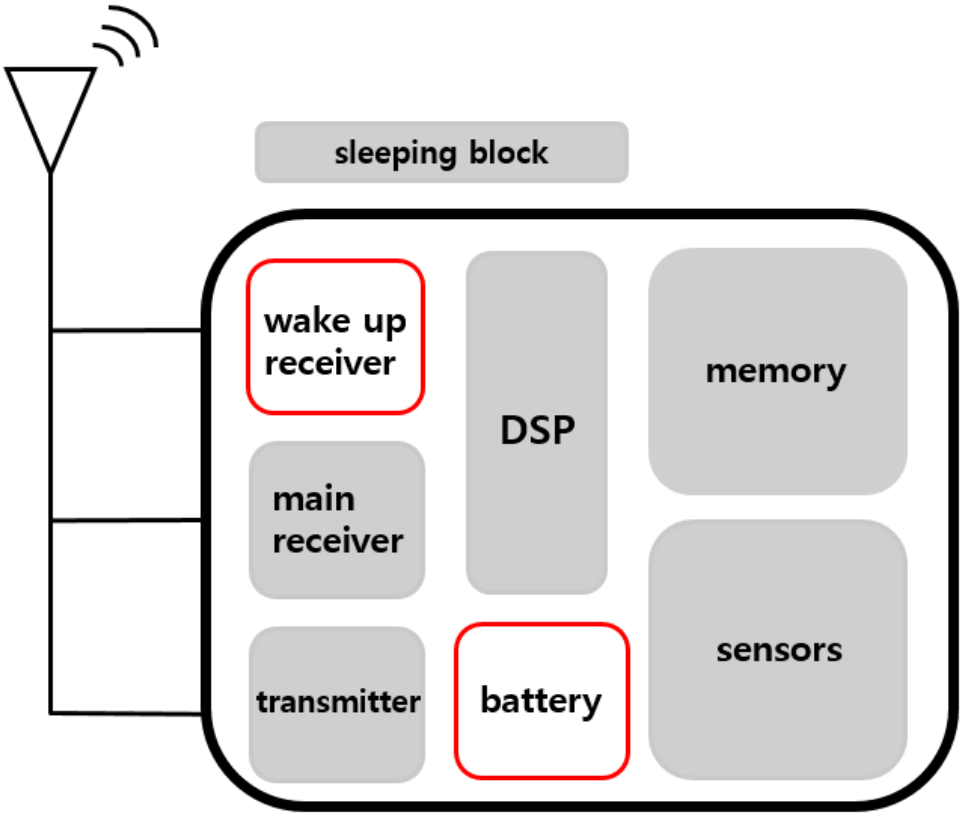

Figure 1.3. The operating block of wake up receiver

operation is shown in Figure 1.2. As a result, the total power consumption can be reduced very much. In this case, global reference clock is necessary to assign time on each node. So the synchronous is impossible and still have quite high power consumption. Second, wake up receiver system is added to main receiver system [2]. The environment of wireless sensor network is shown in Figure 1.1. The wake up receiver is always turned on to receive wake up signal while the other blocks including the main receiver, transmitter, DSP and so on are turned off. This system is shown in Figure 1.3.

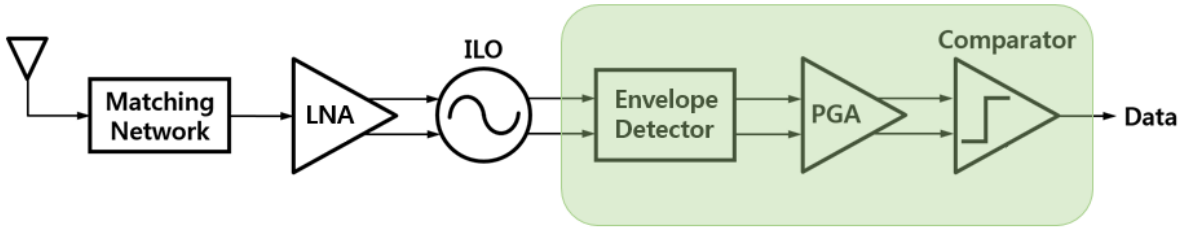

Figure 1.4. The functional block of wake up receiver

For instance, if the wake up receiver take wake up signal, it makes the main receiver turned on. By using this system all node can cut down power consumption significantly.

The functional block of wake up receiver system is shown in Figure 1.4. The wake up signal which is frequency shift keying (FSK) modulated comes from antenna and passes through the matching network. This signal is amplified by using low noise amplifier (LNA) and injected to injection locked oscillator (ILO). Frequency to amplitude conversion of the signal is happened at injection locked oscillator. As a result, the output signal of injection locked oscillator is the shape like amplitude modulated signal. The high frequency signal around 2.4GHz go to baseband signal around 50kHz through envelope detector. Programmable gain amplifier amplifies the signal to suitable size for determining whether this signal is high or low by using comparator. During my master's degree, I focused on the baseband circuits of the wake up receiver especially envelope detector, programmable gain amplifier and comparator.

II. Envelope Detector

The envelope detector is the circuit which takes high frequency input signal and converts the signal into baseband output signal. The main purpose of envelope detector is to extract baseband signal. This envelope detector operates at 2.4GHz. In envelope detector, all transistors are in weak inversion region to exploit exponential transfer and accompany a low-pass filter to obtain the baseband information from the high frequency signal. In this system, fully differential envelope detector [5] is used with replica biasing.

2.1 Conventional envelope detector

The circuit in Figure 2.1 is the conventional envelope detector which is used widely [2, 3]. It is source follower structure envelope detector and there are one transistor which is in weak inversion and low pass filter [4]. The low pass filter consists of a resistor and a capacitor. To get very low cut off frequency, transistor can be used as a resistor. Because saturation region transistor has high resistor value. If nmos transistor is used as shown in Figure 2.1, the cut off frequency can be expressed like

$$f_{cut\ off} = \frac{1}{2\pi \cdot (r_{op} || r_{on}) \cdot C} \ . \tag{1}$$

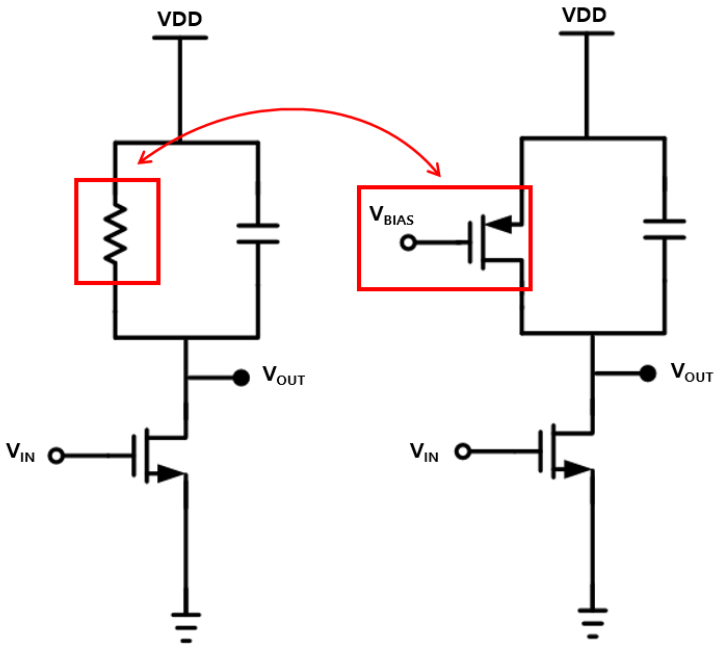

Figure 2.1. Conventional envelope detector

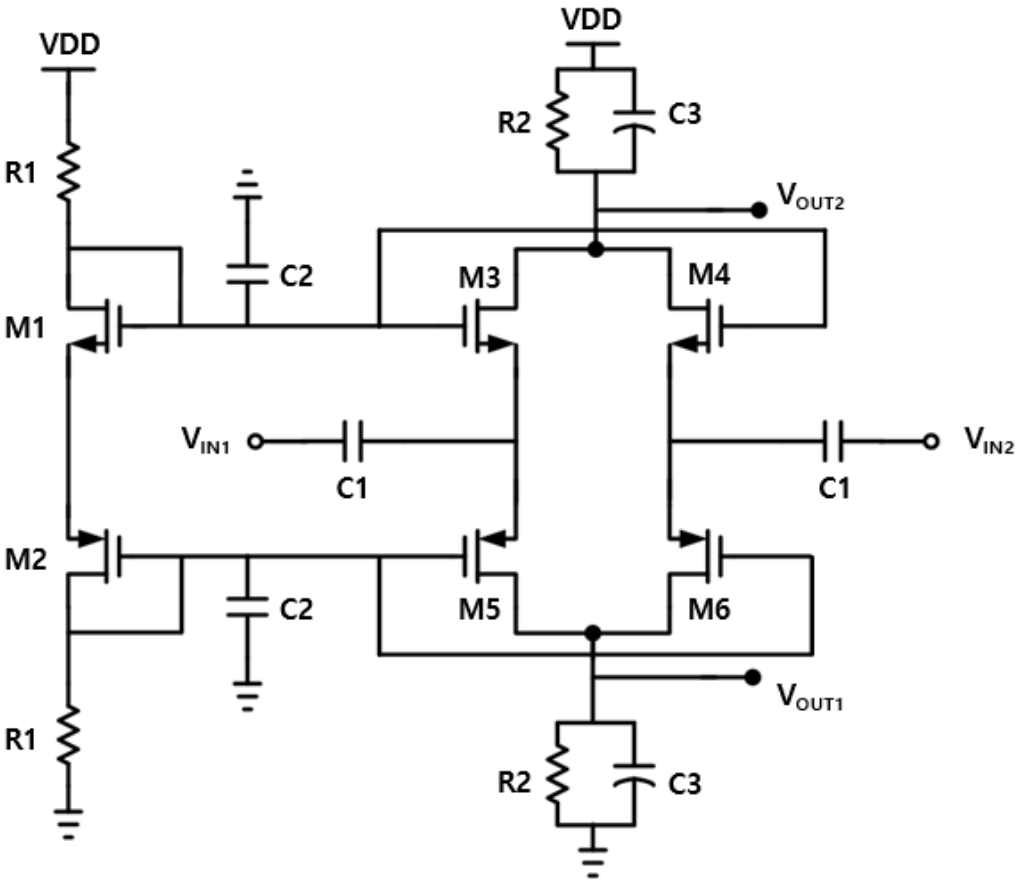

Figure 2.2. Fully differential envelope detector

2.2 Fully differential envelope detector

Fully differential envelope detector is shown in Figure 2.2. It can suppress unwanted low frequency common mode signal through filtering and first-order cancellation. At each input, there is ac coupling capacitor C1 and input impedance of PMOS and NMOS transistors. It acts as high pass filter to filter out the low frequency signal which is under f_{HPF}. As a result, this envelope detector can reject the common mode signal from previous stage. The cut off frequency of high pass filter can be expressed by

$$f_{HPF} = \frac{1}{2\pi\cdot(\frac{1}{g_{m3}}||\frac{1}{g_{m5}}\cdot)C1} \ . \tag{2}$$

This envelope detector consists of two common gate amplifier and low pass filter with resistor and capacitor load in parallel. It is placed on each output node to filter out the high frequency signal. The cut off frequency of low pass filter can be expressed by

$$f_{LPF} = \frac{1}{2\pi\cdot R2\cdot C3} \ . \tag{3}$$

A replica biasing circuit is added to grab the biasing point strongly. The M3, M4, M5 and M6 have nonlinear characteristic. The input signal is injected to the source nodes and the output signal is get from the drain nodes.

The drain current equation for M1 is given by [6]

$$I_{d,M1} = I_0 e^{\frac{V_G - V_{th}}{nV_T}} [e^{\frac{-V_S}{V_T}} e^{\frac{-vi^+}{V_T}} - e^{\frac{-V_D}{V_T}}] \tag{4}$$

$$I_0 e^{\frac{V_G - V_{th}}{nV_T}} e^{\frac{-V_S}{V_T}} = I_Q$$

$$I_{d,M1} = I_Q e^{\frac{-vi^+}{V_T}} \ .$$

I_Q is the static current, V_T is the thermal voltage which is *kT/q* and V_{th} is the threshold voltage of transistor. n reduces the slope of transfer function for losses because of capacitive division. The small signal current of common source and source follower topologies is given by

$$I_{d,M1} = I_Q e^{\frac{vi^+}{nV_T}} \ . \tag{5}$$

Comparing (1) and (2), common gate topology has advantage in small signal current which is efficient nonlinear transfer than common source and source follower topologies. Because there is no n in common gate topology but common source and source follower have n which is larger than 1.5.

By using Taylor series, the second order term of the small signal baseband current can be get

$$I_{d,M1} = I_Q[\ \frac{e^0}{0!} + \frac{e^0}{1!}\left(\frac{-v_i}{V_T}\right) + \frac{e^0}{2!}\left(\frac{-v_i}{V_T}\right)^2 + \ \cdots\ ] \tag{6}$$

$$= I_Q[\ 1 - \frac{{v_i}^+}{V_T} + \frac{{v_i}^{+2}}{2{V_T}^2} - \ \cdots\ ] \ .$$

The second order term is expressed by

$$I_{d,M1,second\ order\ term} = \frac{I_Q {v_i}^{+2}}{2{V_T}^2} \ . \tag{7}$$

For example, if the input signal is $v_i{}^+ = Asin(2\pi f_{in}t) = v_p \sin(2\pi f_{in}t)$ at high frequency, when v_p is the peak voltage value of input signal, the baseband output current can be calculated as

$$I_{d,M1,second\ order\ term} = \frac{I_Q {v_p}^2 sin^2(2\pi f_{in}t)}{2{V_T}^2} \tag{8}$$

$$= \frac{I_Q {v_p}^2}{2{V_T}^2} \times \frac{1 - \cos(4\pi f_{in}t)}{2}$$

$$= \frac{I_Q {v_p}^2 - I_Q {v_p}^2 \cos(4\pi f_{in}t)}{4{V_T}^2} \ .$$

After low pass filtering, only low frequency signal is remained and the total current is doubled, which is

$$I_o = \frac{I_Q {v_p}^2}{4{V_T}^2} \times 2 = \frac{I_Q {v_p}^2}{2{V_T}^2} \ . \tag{9}$$

As a result, the total output voltage is given by

$$V_o = \frac{I_Q {v_p}^2 R_2}{2{V_T}^2} \ . \tag{10}$$

A same analysis can be done for PMOS. When the input signal is injected, the Vout1 voltage level go high, adversely the Vout2 voltage level go low because of the charge flow. In conclusion the differential output voltage amplitude can be calculated as

$$V_{od} = \frac{I_Q {v_p}^2 R_2}{2{V_T}^2} \times 2 = \frac{I_Q {v_p}^2 R_2}{{V_T}^2} \ . \tag{11}$$

The component values are summarized in Table 1, which are used in fully differential envelope detector design. From specific value, the cut off frequency of the low pass filter and high pass filter can be calculated as

$$f_{HPF} = \frac{1}{2\pi RC} = \frac{1}{2\pi C_1 (\frac{1}{g_{nmos}} || \frac{1}{g_{pmos}})} = 30\text{MHz} \tag{12}$$

$$f_{LPF} = \frac{1}{2\pi RC} = \frac{1}{2\pi C_3 R_2} = 531\text{kHz} \ .$$

Components	**Specification**	**Value**	**Unit**
VDD	Voltage	1.8	V
M1, M3, M4	Width/Length	3/0.2	μm/μm
M2, M5, M6	Width/Length	6/0.2	μm/μm
R1	Resistance	600	kΩ
R2	Resistance	300	kΩ
C1	Capacitance	100	fF
C2	Capacitance	1	pF
C3	Capacitance	1	pF

Table 1. The component values for fully differential envelope detector

2.3 Conversion gain of fully differential envelope detector

Conversion gain is important property for envelope detector. We want to get the output signal without signal loss. It means that the down conversion efficiency from high frequency signal to low frequency signal is significant to this system. The conversion gain of this fully differential envelope detector can be expressed as

$$\frac{V_o}{V_{in}} = \frac{\frac{I_Q {v_p}^2 R_2}{2{V_T}^2}}{V_p} = \frac{I_Q v_p R_2}{2{V_T}^2} \quad . \tag{13}$$

The conversion gain is shown in Figure 2.4. Figure 2.5 is the graph for getting specific amplitude value of Vin and Vout. The value of conversion gain has one when v_p is 55mV. It indicates that if the input signal is less than 55mV, the output signal is degraded than the input signal. Adversely if the input signal is higher than 55mV, the output signal is larger than the input signal like Figure 2.3. For example, when we need to compare two signal, one is under 55mV the other one is upper 55mV. In this system, this kind of envelope detector is suitable. The envelope detector has good conversion gain while the total static current consumption is 2.25μA.

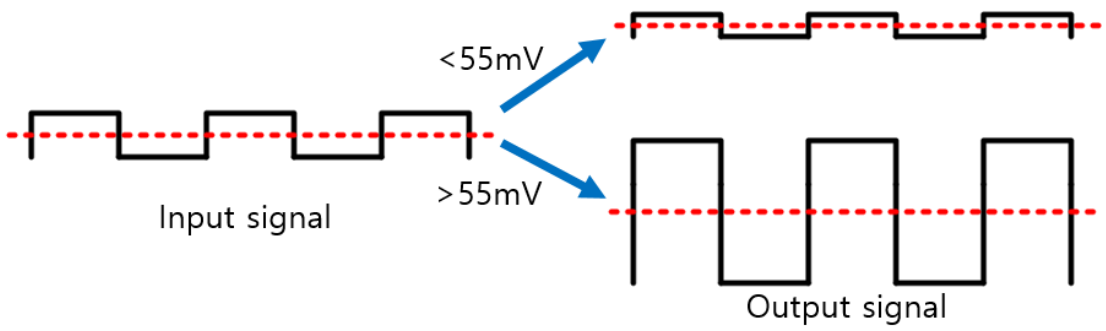

Figure 2.3. Comparing input and output signal amplitude

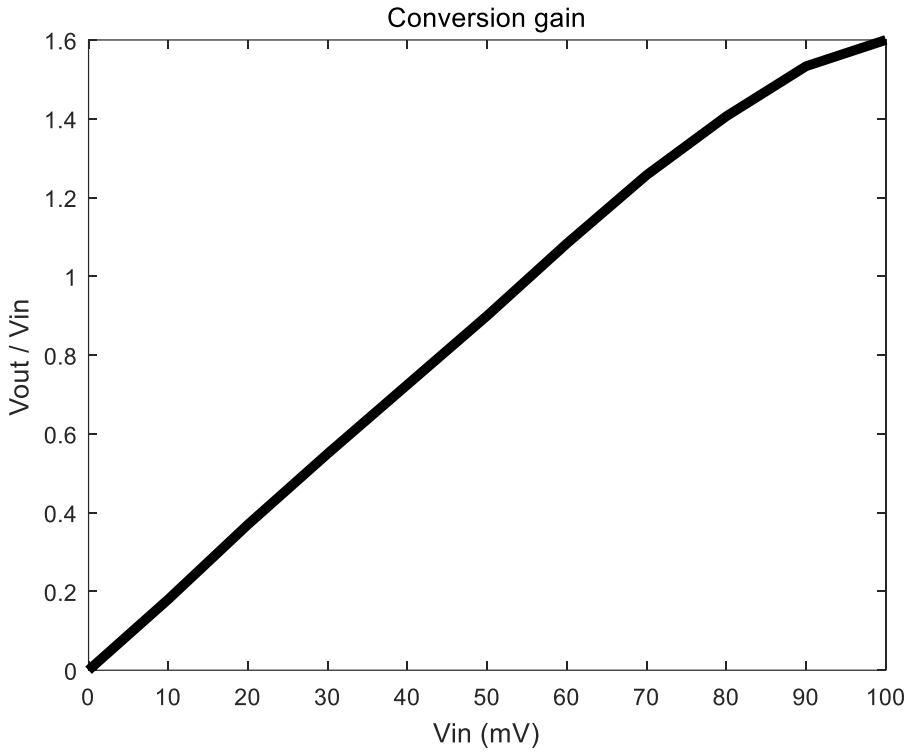

Figure 2.4. Conversion gain of fully differential envelope detector

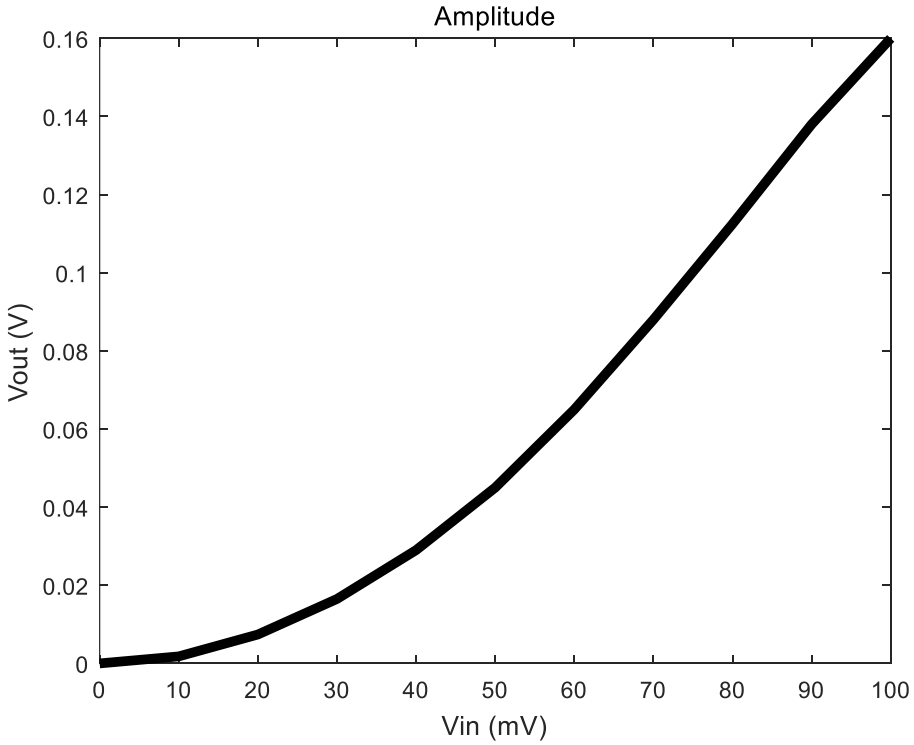

Figure 2.5. Output signal amplitude value on each Vin

III. Programmable Gain Amplifier

The output signal of envelope detector is amplified through programmable gain amplifier. Programmable gain amplifier consists of fully differential amplifier structure with feedback network. In this programmable gain amplifier, the gain can be controlled 5V/V, 10V/V, 15V/V and 20V/V by using capacitive feedback.

3.1 Operational trans-conductance amplifier

The first step of designing programmable gain amplifier is understanding about operational trans-conductance amplifier. Two stage configuration is the most widely used for the implementation shown in Figure 3.1.

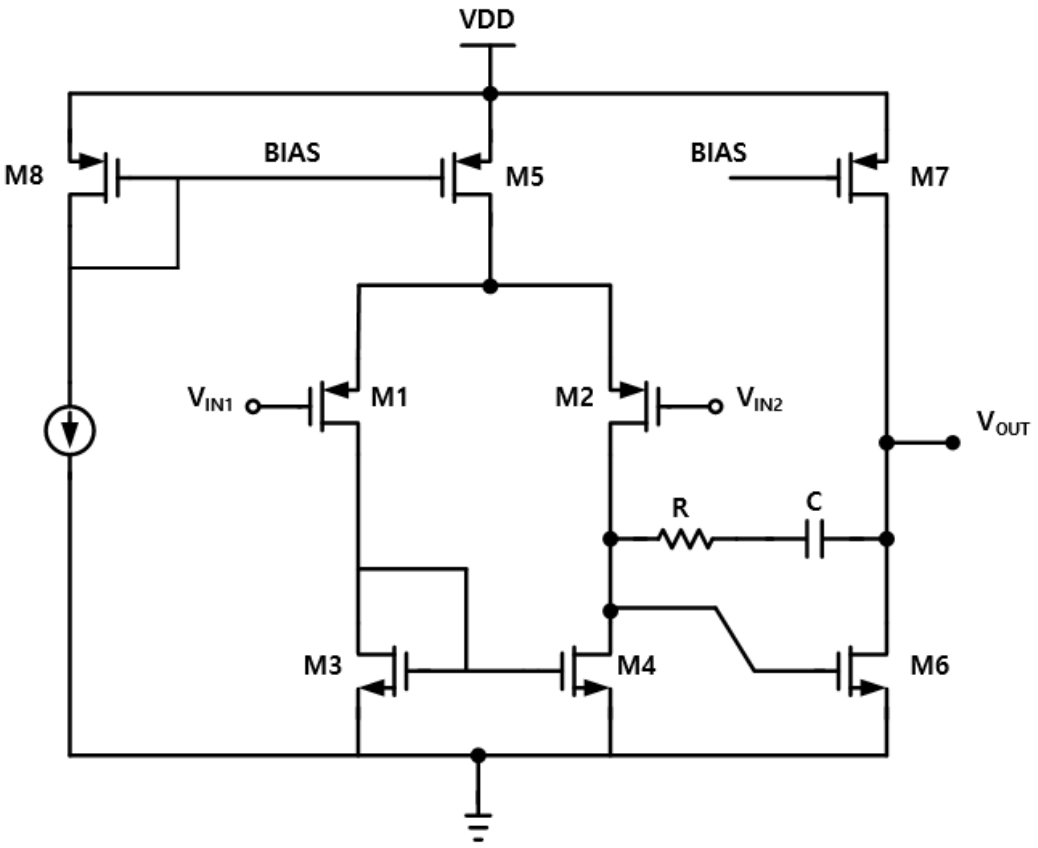

Figure 3.1. Two stage operational amplifier

The first stage consists of PMOS transistors and NMOS transistors which act as loads. The current is from the current source of PMOS transistor. The second stage is also common source structure. Let's assume that the voltage value of V_{IN2} is reference voltage, for instance the value is VDD/2. If there is input voltage difference between M1 and M2, the current through M1 and M2 is different. It makes the gain. The first stage gain can be expressed by

$$A_{v,1st} = -\mathrm{g_{m1}}(r_{o2}||r_{04}) \ . \tag{14}$$

And the second stage gain is

$$A_{v,2nd} = -\mathrm{g_{m6}}(r_{o6}||r_{07}) \ . \tag{15}$$

As a result, the total gain can be calculated as

$$A_{v,total} = \mathrm{g_{m1}}(r_{o2}||r_{04}) \cdot \ \mathrm{g_{m6}}(r_{o6}||r_{07}) \ . \tag{16}$$

There are 2 poles in this topology. The first pole is located in the first stage output and the second pole is at the second stage output. Basically 2 poles mean 180° phase shift between input and output. If the phase margin is less than 45° the output signal can be oscillated easily. It makes a stability issue. To avoid this problem, the capacitor is added between the first stage output and the second stage output [7]. If the capacitor is put, the dominant pole is going to origin while the second pole is going to outside. It called pole splitting [8].

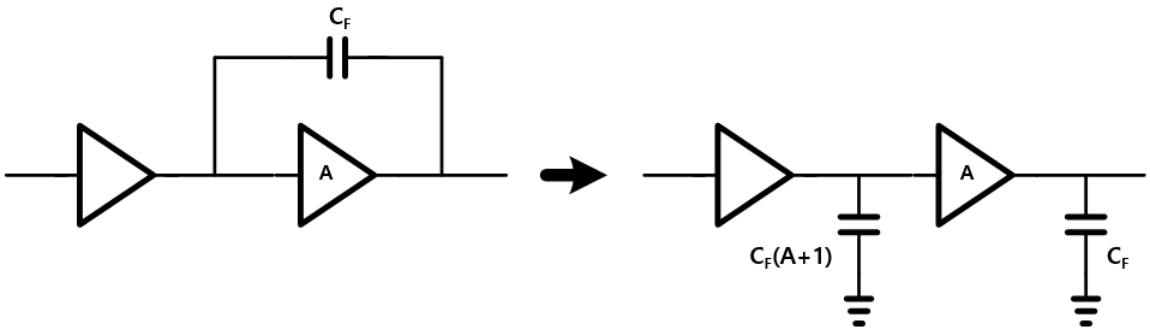

Figure 3.2. Miller theorem

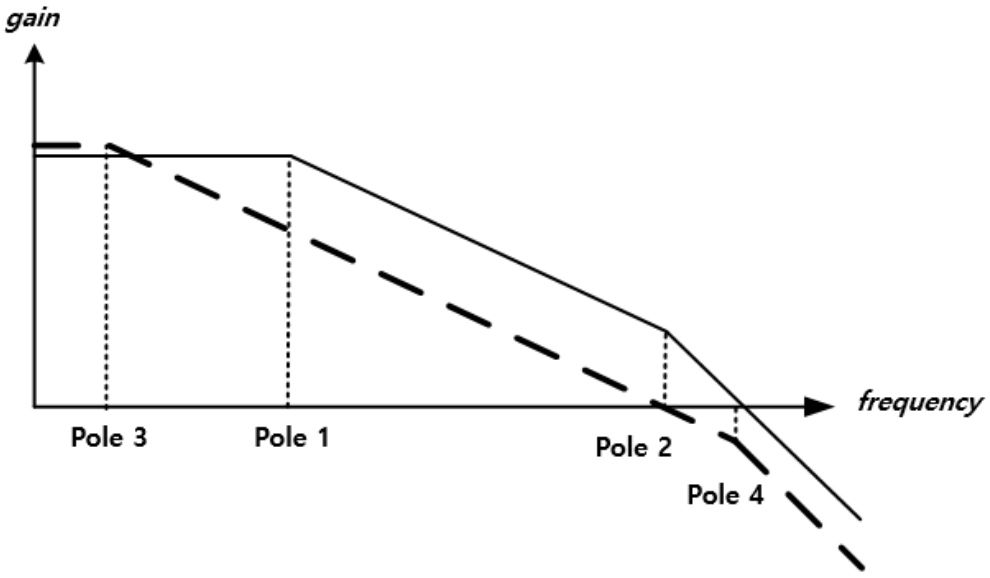

Figure 3.3. Pole splitting

As shown in Figure 3.3, pole 1 and pole 2 are the poles before adding the compensation capacitor. In this schematic, the phase margin is lower than 0. After putting the compensation capacitor the poles are split like pole 3 and pole 4. As a result we can get reliable phase margin around 60°.

Physically, the zero comes from the compensation capacitor which serves a path for the high frequency signal to go directly from the gate to the drain though the compensation capacitor. In Figure 3.1 the high frequency signal can move from the gate node to the drain node of M6 without inversion, while the signal inversion is happened at low frequency through M6. It causes stability degrade. Many paper have analyzed about the circuit in Figure 3.1 [9]. The zero location is

$$z = \frac{1}{C(\frac{1}{g_{m6}} - R)} \quad . \tag{17}$$

To eliminate right half plane zero, a nulling resistor in inserted in series with compensation capacitor like R and C in Figure 3.1. The nulling resistor value is

$$R = \frac{1}{g_{m6}} \quad . \tag{18}$$

3.2 Fully differential amplifier

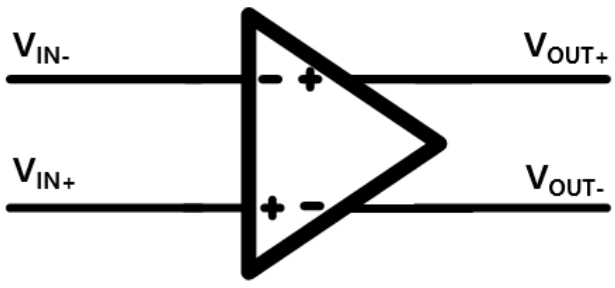

Figure 3.4. Fully differential amplifier structure

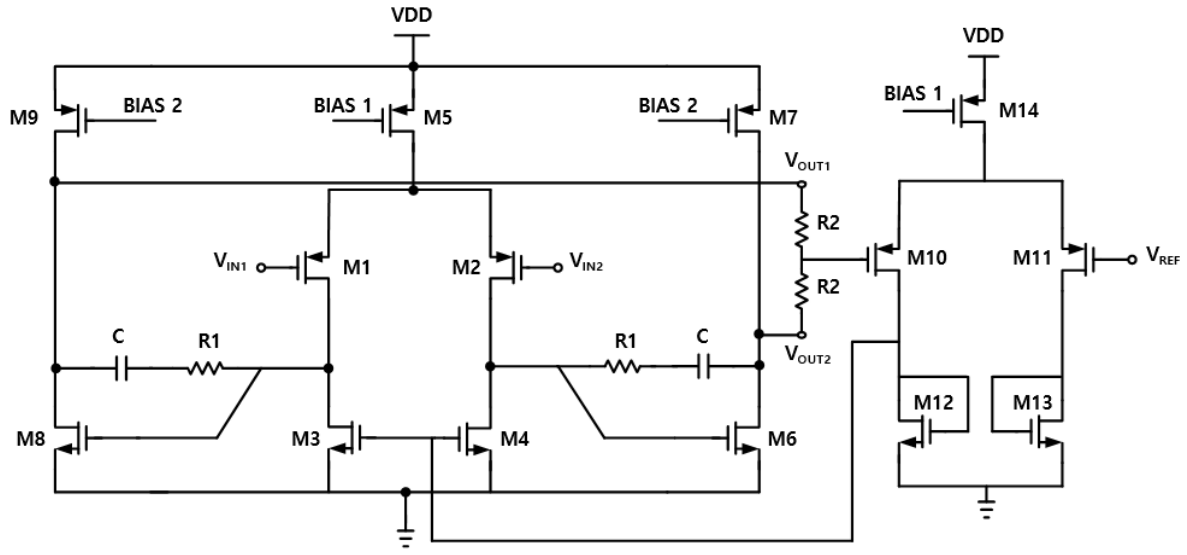

Figure 3.5. Fully differential amplifier schematic with common mode feedback

This wake up receiver baseband system is fully differential structure. By accompanying fully differential structure, this system is robust from environment noise and ac coupling noise. This structure has two inputs and two outputs in Figure 3.4 and Figure 3.5. In fully differential amplifier, common mode feedback is necessary [10]. If there is no common mode feedback, the transistors as load and current source may enter triode region easily. When we design fully differential amplifier, we should care about common mode feedback stability and differential feedback stability. Fortunately, the stability can be checked by using simulation. Figure 3.6 is the simulation result for loop gain and phase margin of common mode feedback loop. I use two resistors to sense differential outputs. Moreover, when we design the amplifier which is in common mode feedback loop, carefully think which topology is suitable. If the amplifier has large gain, it is hard to get enough phase margin. That's why I chose diode connected amplifier topology which has low gain comparing single ended operational amplifier.

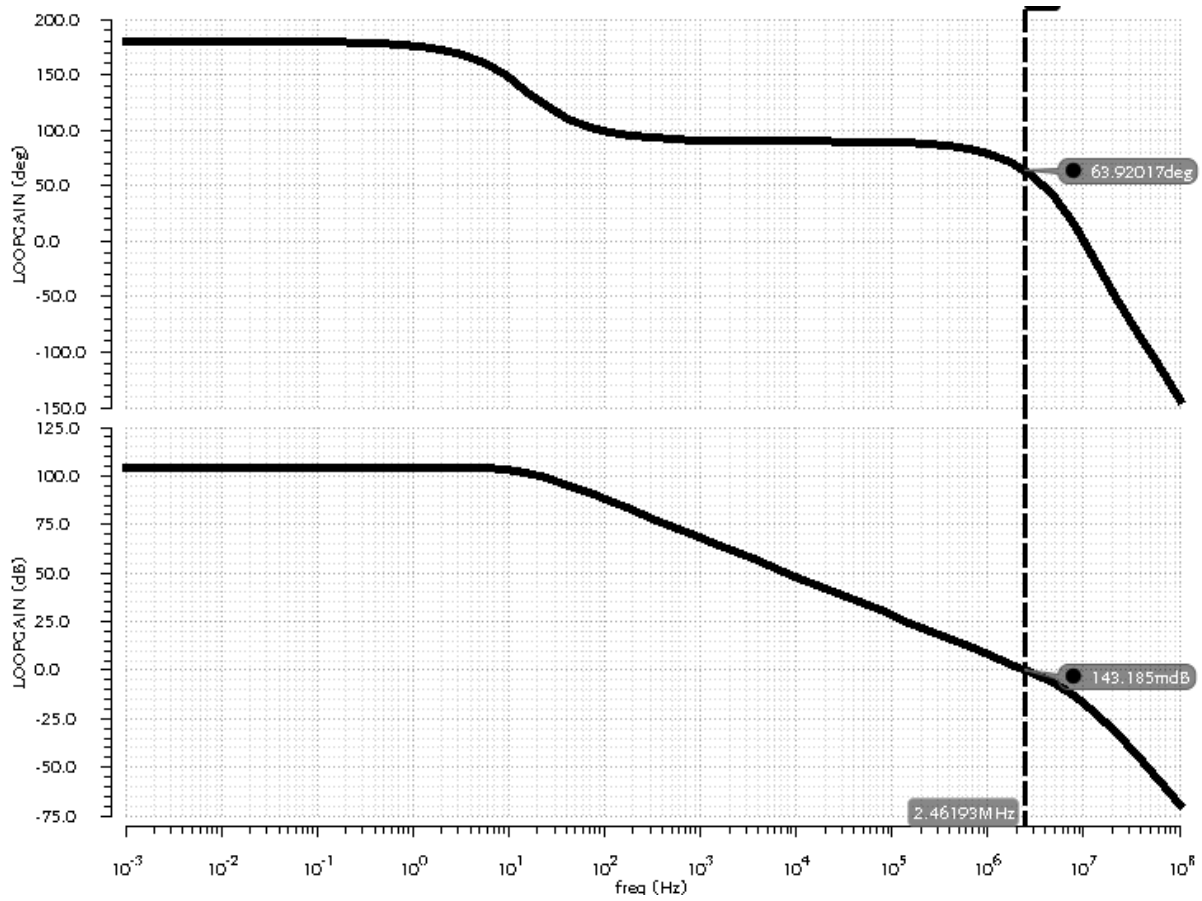

Figure 3.6. Loop gain and phase margin of common mode feedback loop

3.3 Resistive feedback

When we design programmable gain amplifier, negative feedback network is necessary. Figure 3.7 shows feedback structure of programmable gain amplifier. A is open loop gain and β is feedback factor. From Figure 3.5, the open loop gain can be expressed like

$$A = g_{m2}(r_{o2}||r_{o4}) \cdot g_{m6}(r_{o6}||r_{o7}). \tag{19}$$

In Figure 3.7, feedback factor β is expressed by

$$\beta = \frac{R_1}{R_1+R_F} \ . \tag{20}$$

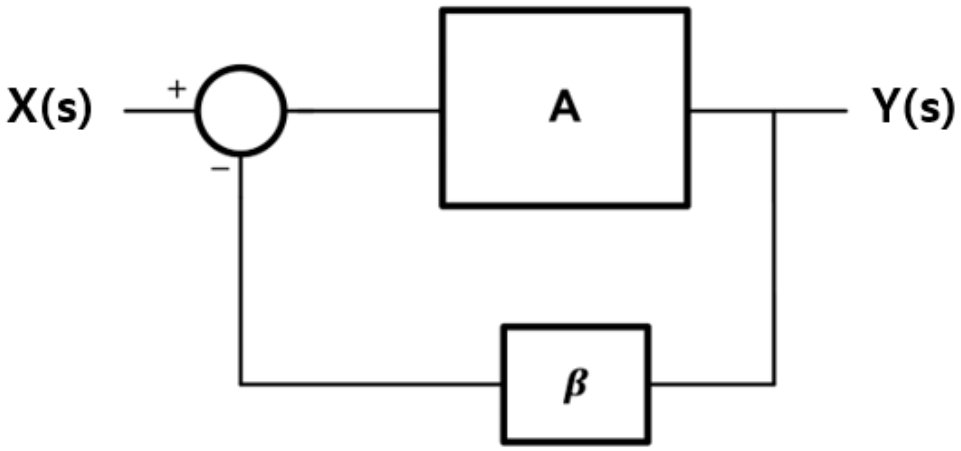

Figure 3.7. Feedback topology of programmable gain amplifier

The close loop gain is

$$\frac{Y(s)}{X(s)} = \frac{A}{1+A\beta} \quad . \tag{21}$$

If $A\beta$ is very large ($A\beta \gg 1$), close loop gain can be approximately calculated like

$$\frac{Y(s)}{X(s)} = \frac{A}{1+A\beta} \approx \frac{1}{\beta} = 1 + \frac{R_F}{R_1(R_2,R_3,R_4)} \cong \frac{R_F}{R_1(R_2,R_3,R_4)} \quad . \tag{22}$$

The gain of programmable gain amplifier can be controlled by using resistor feedback in Figure 3.8. The gain of this system is 5V/V, 10V/V, 15V/V. 20V/V. R_F is 300kΩ and the gain control resistor is 15kΩ, 20kΩ, 30kΩ and 60kΩ. By using switch, the gain can be chosen.

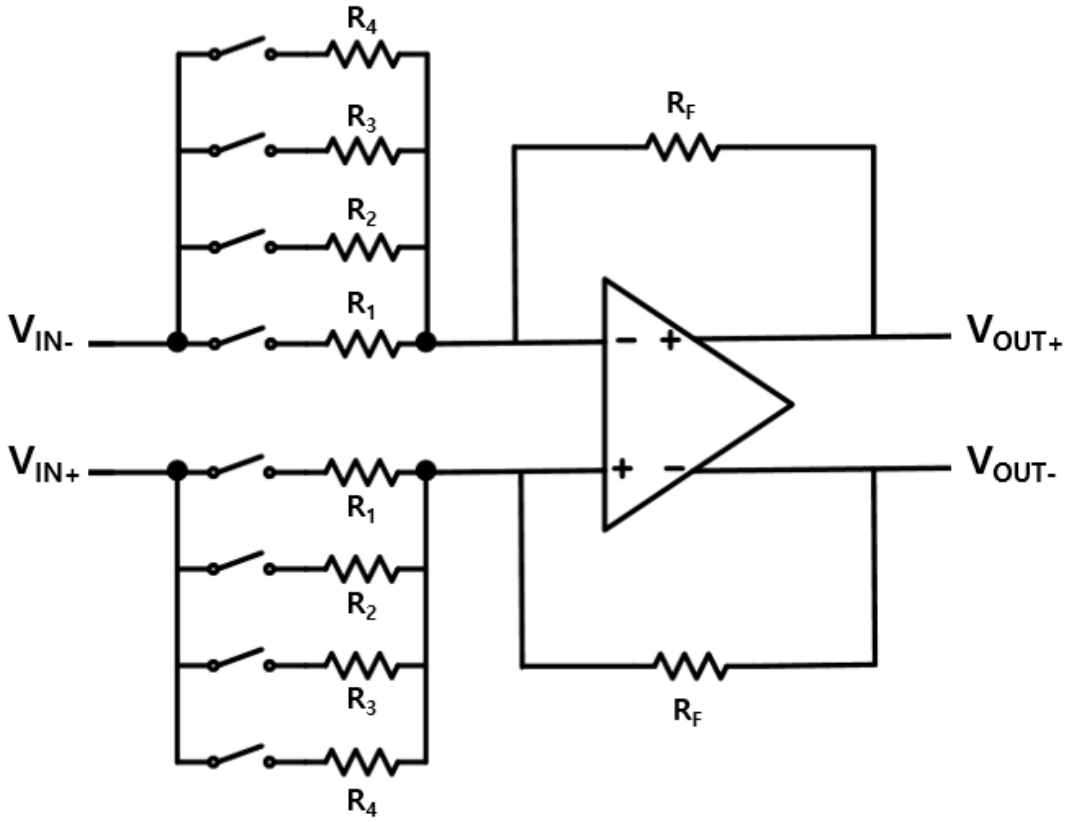

Figure 3.8. Programmable gain amplifier with resistor feedback

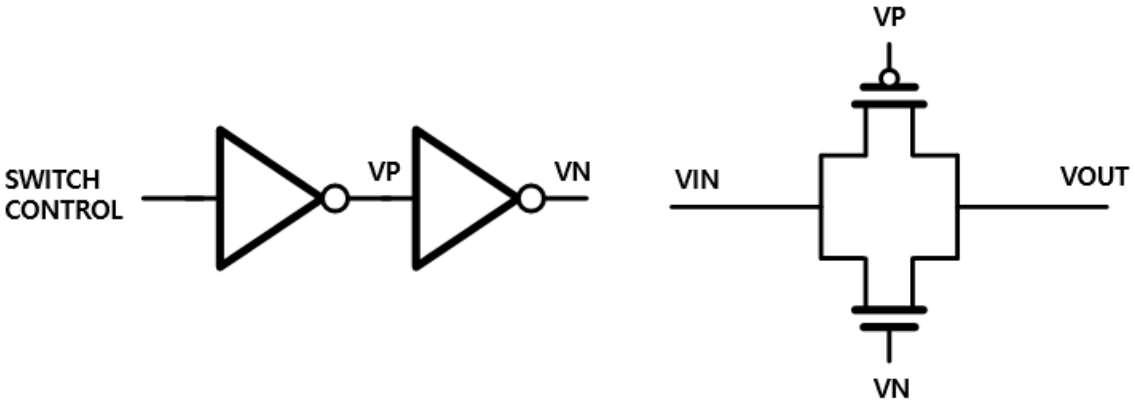

Figure 3.9. Control topology and CMOS switch

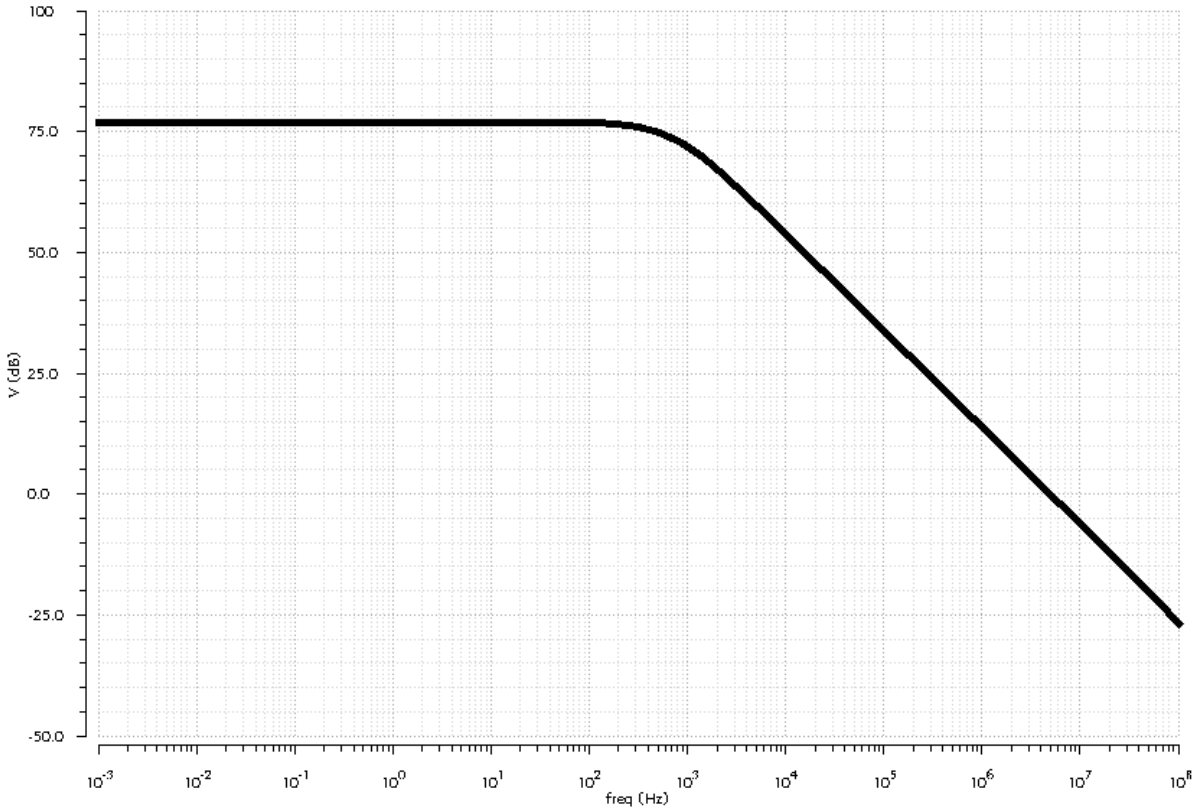

Figure 3.10. Open loop gain simulation result

R_F	300kΩ
R_1	60kΩ
R_2	30kΩ
R_3	20kΩ
R_4	15kΩ

Table 2. Resistor value of negative feedback network

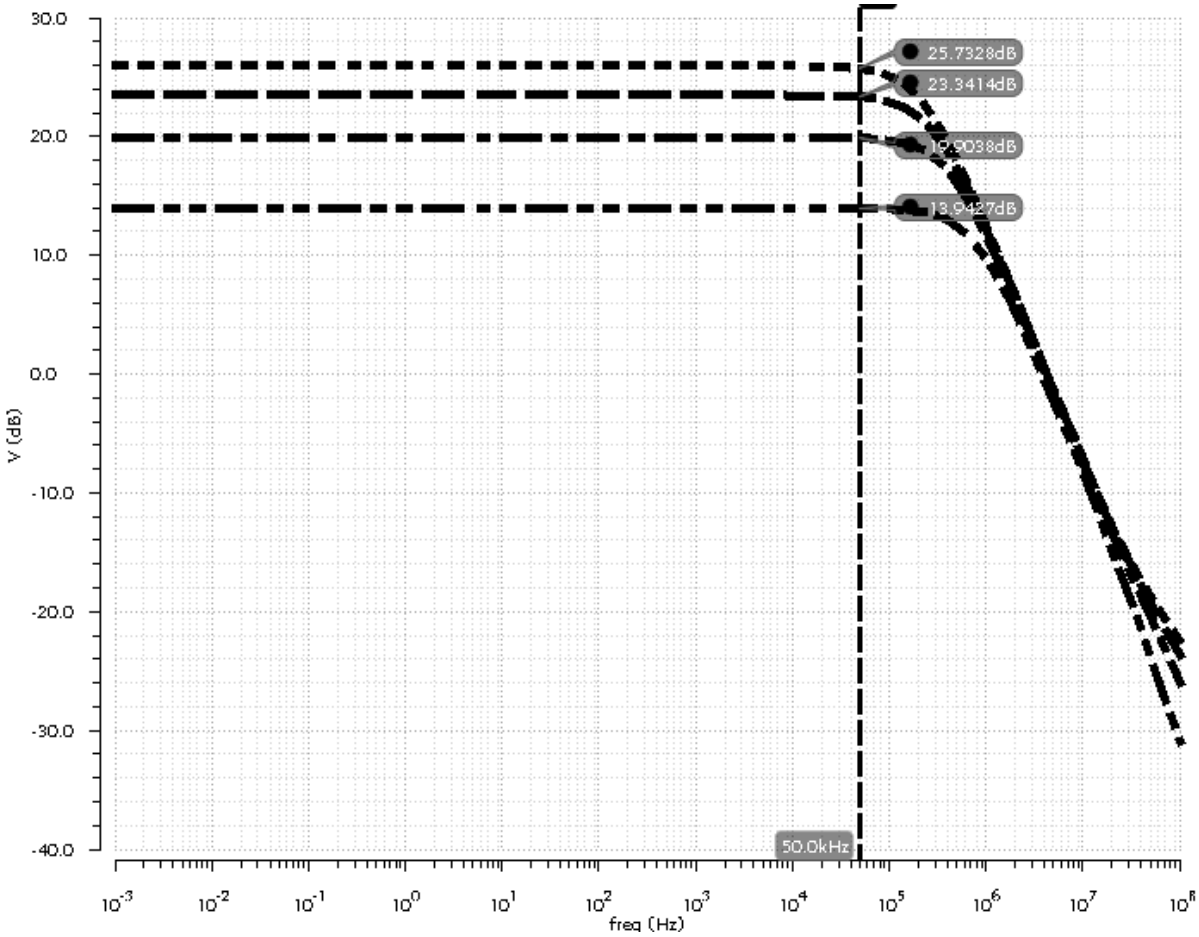

Figure 3.11. Frequency response of programmable gain amplifier with resistive feedback (5V/V, 10V/V, 15V/V and 20V/V)

The CMOS switch is designed like Figure 3.9. The switch is controlled by two inverters. When the SWITCH CONTROL is high, the switch is on and when the SWITCH CONTROL is low, the switch is off.

To maximize speed, minimum length which is 180nm is used and the width is 220nm, 440nm for NMOS and PMOS each to degrade clock noise like charge injection and clock feedthrough. If the width is large, parasitic capacitor value of the switch is large also. It causes more switching noise however, turn on resistor of switch is lower than small size switch.

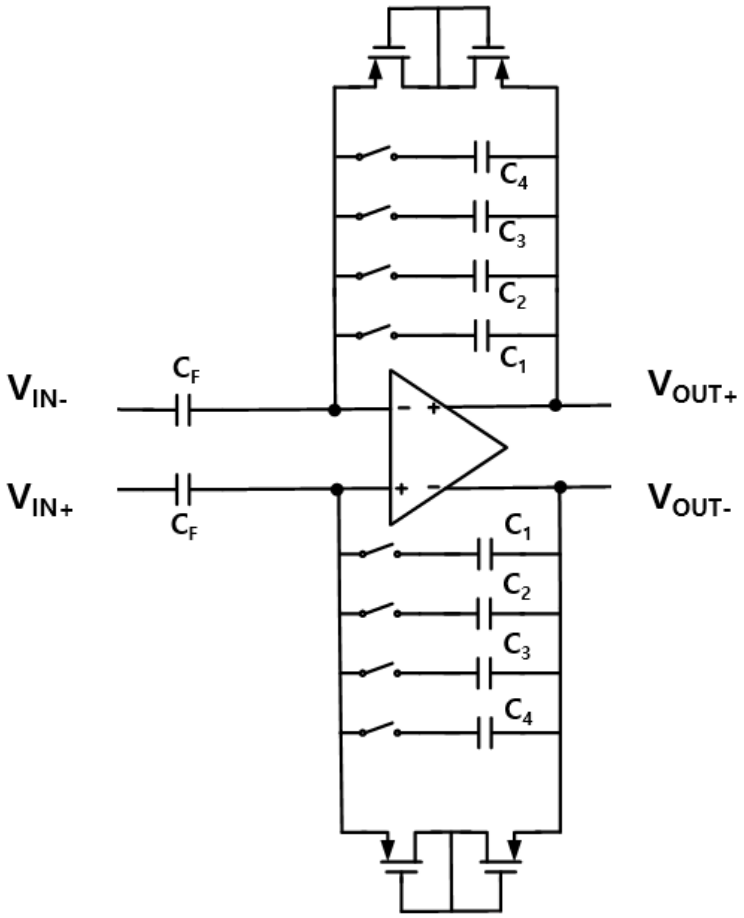

Figure 3.12. Programmable gain amplifier with capacitive feedback

3.4 Capacitive feedback

Capacitive feedback also can be used in programmable gain amplifier. But, in this schematic pseudo resistor is necessary to do biasing input and output [11]. Because if there is only capacitor between input and output, capacitor block dc signal. It makes a problem of biasing. Pseudo resistor can be designed by using diode connected PMOS. It has very high impedance. The length is 1μm and the width is 400nm. The capacitive feedback network with pseudo resistor structure is shown in Figure 3.12. Figure 3.13 is the frequency response of programmable gain amplifier when the gain is 5/V, 10V/V, 15V/V and 20V/V.

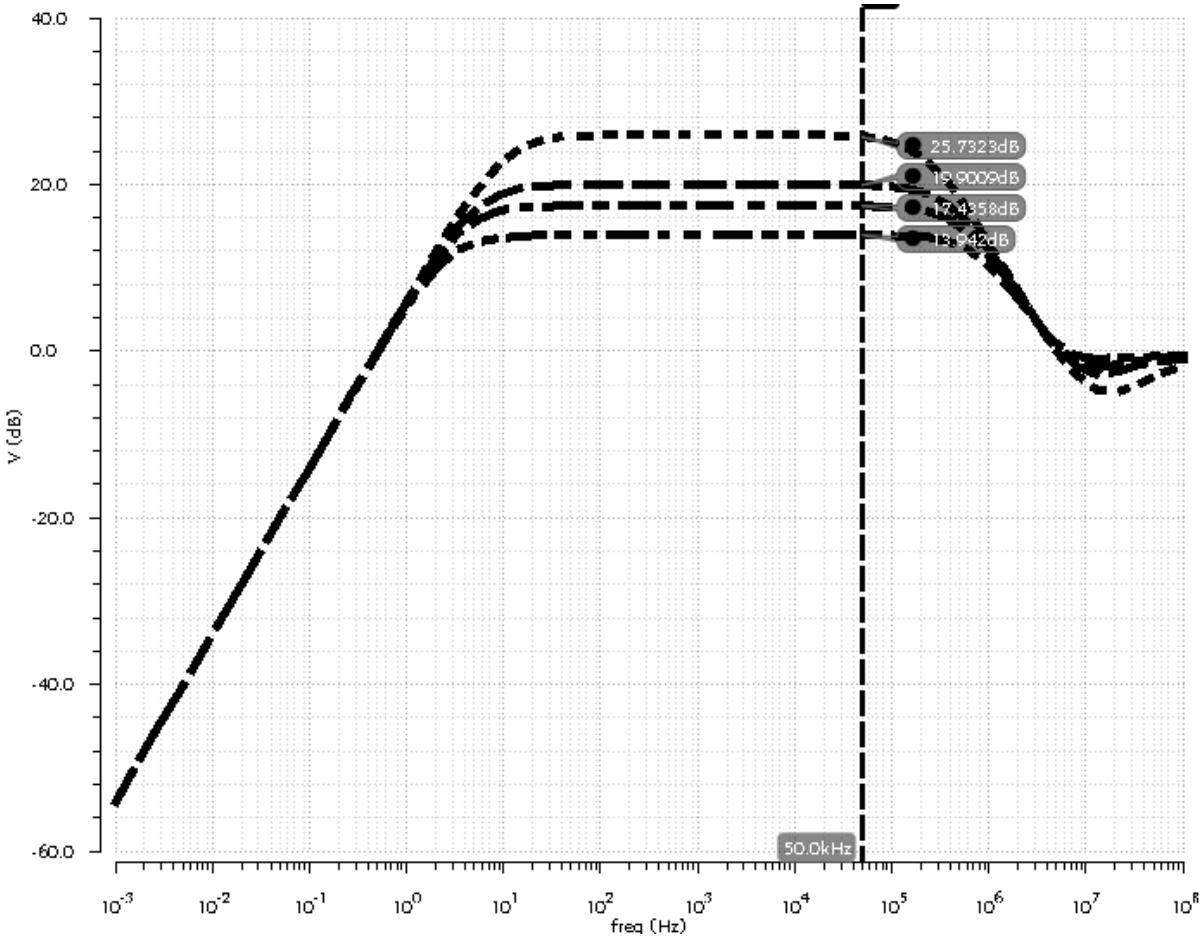

Figure 3.13. Frequency response of programmable gain amplifier with resistive feedback

(5V/V, 10V/V, 15V/V and 20V/V)

C_F	3pF
C_1	600fF
C_2	300fF
C_3	200fF
C_4	150fF

Table 3. Capacitor value of negative feedback network

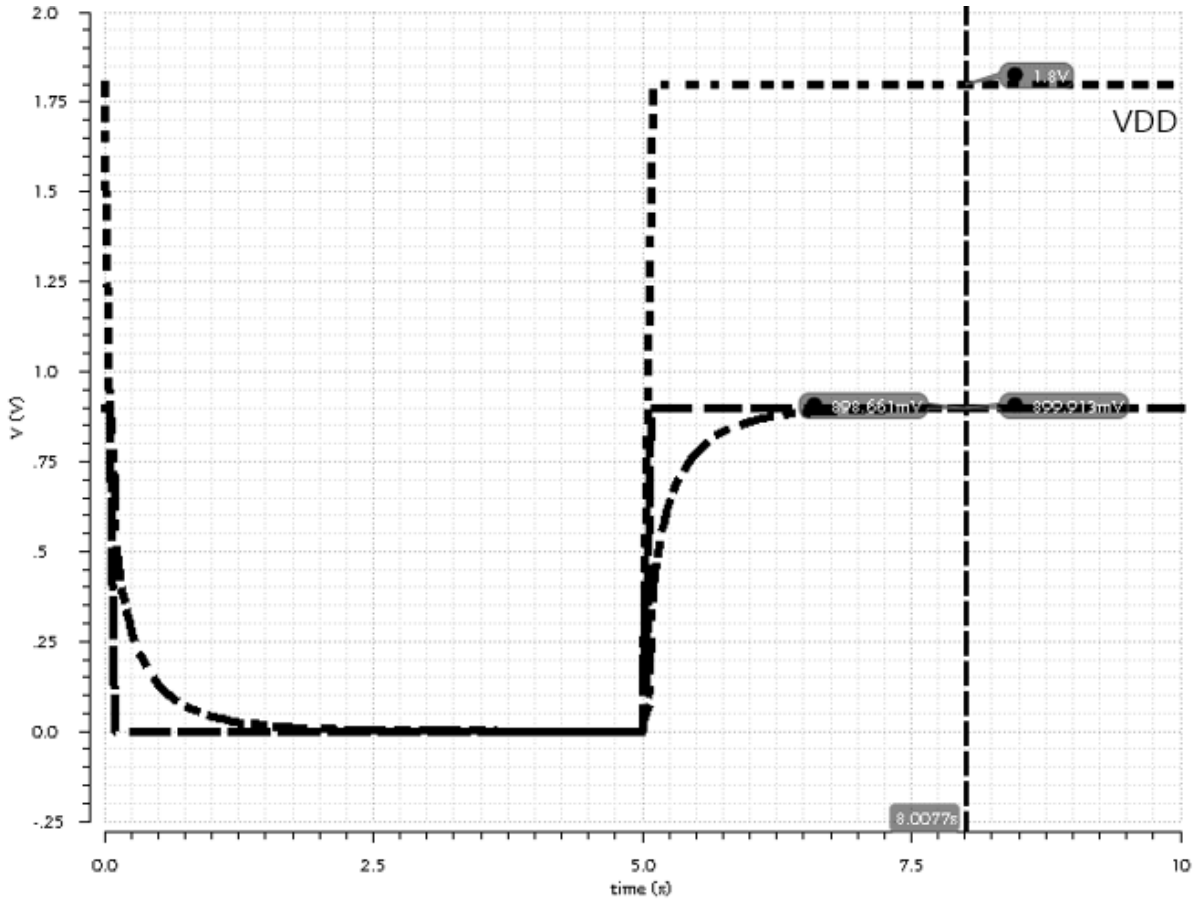

Figure 3.14. Stability check by using transient simulation

In Figure 3.6, we simulated common mode loop gain and phase margin. After adding the capacitance feedback network, we have to check the stability one more. The stability can be confirmed through transient simulation in Figure 3.14. When the 1.8V supply voltage signal which is dot line is injected to this circuit at 5 seconds, the output signal which is dash line can follow to VDD/2 without much oscillation. The dash-dot line is the node voltage which is between the input capacitance and the input transistor. This signal also can follow to half VDD well.

3.5 Noise analysis

In this system, two stage op amp is used. To get input referred thermal noise, noise analysis is required. Second stage input referred thermal noise can be calculated like

$$\overline{V_n^2}|_{M5\sim8} = 2 \times 4\text{kT}\gamma(g_{m5} + g_{m7})(r_{o5}||r_{o7})^2 \times \frac{1}{g_{m1}^2(r_{o1}||r_{o3})^2 g_{m5}^2(r_{o5}||r_{o7})^2}$$

$$= 8kT\gamma \frac{g_{m5}+g_{m7}}{g_{m1}^2 g_{m5}^2(r_{o1}||r_{o3})^2} \ . \quad (23)$$

The noise due to M1 ~ M4 is calculated as

$$\overline{V_n^2}|_{M1\sim4} = 2 \times 4kT\gamma \frac{g_{m1}+g_{m3}}{g_{m1}^2} \ . \quad (24)$$

In conclusion, the total input referred thermal noise is

$$\overline{V_n^2}|_{total} = 8kT\gamma \frac{1}{g_{m1}^2}\left[g_{m1} + g_{m3} + \frac{g_{m5}+g_{m7}}{g_{m1}^2 g_{m5}^2(r_{o1}||r_{o3})^2}\right] \ . \quad (25)$$

From these result, we can know that second stage is usually negligible because it is divided by the total gain. In two stage op amp, first stage noise is dominant.

3.6 Apply chopper stabilization technique

Noise parameter is one of the important factors when we design programmable gain amplifier. There are two dominant noise which have to be considered. One is the thermal noise, the other one is the flicker noise. The thermal noise is the white noise over all frequency band and the flicker noise depends on the frequency value. Moreover, the dc offset is a big problem

so that we need to eliminate noise and dc offset. To eliminate noise perfectly is impossible but we can design amplifier which have low noise and cut out dc offset relatively by employing chopper stabilization technique [12]. The amplifier with chopper stabilization technique remain the white noise characteristic, but can remove its input offset and flicker noise. The chopper stabilization structure is shown in Figure 3.15.

Figure 3.15 (a) is the chopper stabilization structure which is composed of 4 switches. The switch is same size with Figure 3.9. Figure 3.15 (b) is the symbol of chopper stabilization. The M1, M2, M3 and M4 of the programmable gain amplifier in Figure 3.5 are dominant transistors in noise analysis. From this result, the chopper structure is put between the input of first stage and the output of first stage.

Usually we can get output noise in measurement. But, engineer want to figure out the input noise which is called the input referred noise. The value of input referred noise can be calculated from the output noise dividing by the gain. The reason why the input referred noise is carefully considered is that if the input referred noise is larger than input signal, the amplifier is meaningless.

Figure 3.16 shows the comparison of input referred noise when the chopper circuit is applied and without chopper stabilization technique. The upper line is the programmable gain amplifier without chopper circuit and the below line is with chopper circuit. Obviously the amplifier with chopper circuit can reduce the noise 20 times lower than the other amplifier without chopper circuit.

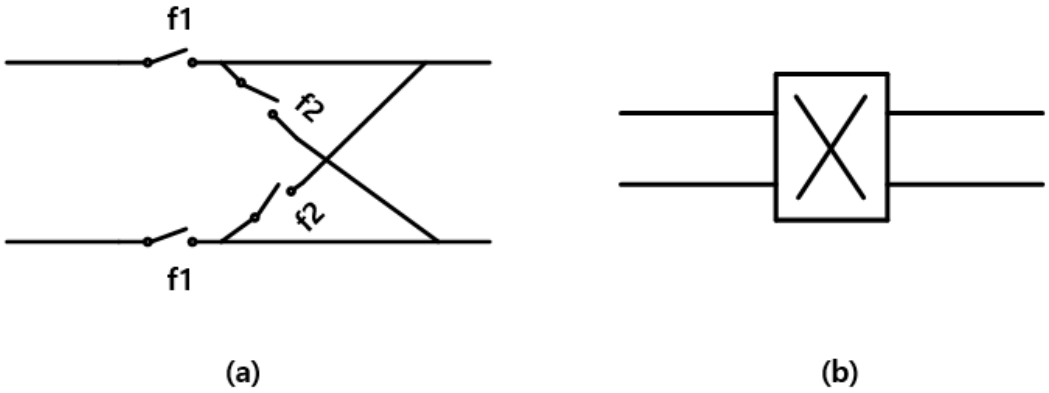

Figure 3.15. (a) Chopper stabilization structure (b) Symbol of chopper stabilization

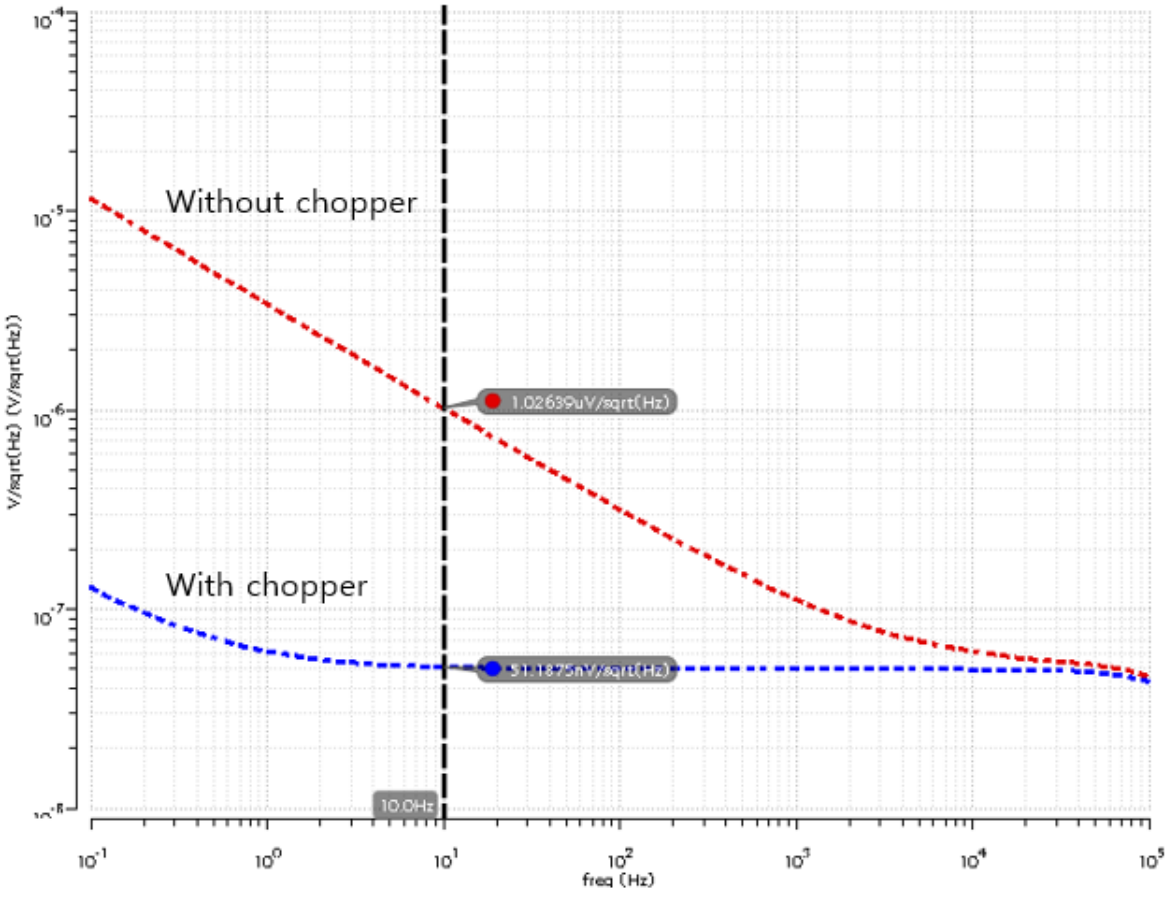

Figure 3.16. Comparison of input referred noise without chopper stabilization technique and with chopper stabilization technique at 10Hz

Gain	Bandwidth	Integrated input referred noise
5V/V	17Hz ~ 840kHz	94μV
10V/V	34Hz ~ 440kHz	68μV
15V/V	51Hz ~ 295kHz	57μV
20V/V	65Hz ~ 255kHz	50μV

Table 4. Programmable gain amplifier Gain, Bandwidth and Integrated input referred noise

IV. Comparator

The comparator is essential circuit that compare one signal with a reference voltage or another analog signal. In this system, the comparator compares the differential output signal of the programmable gain amplifier.

4.1 Threshold inverter quantizer

The threshold inverter quantizer (TIQ) is shown in Figure 4.1. This comparator consists of two inverters. First stage inverter and second stage inverter should same. The input signal is compared with internal threshold voltage of inverter. The threshold voltage of inverter can be expressed as [13]

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{DD} - |V_{tp}|)}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad . \tag{26}$$

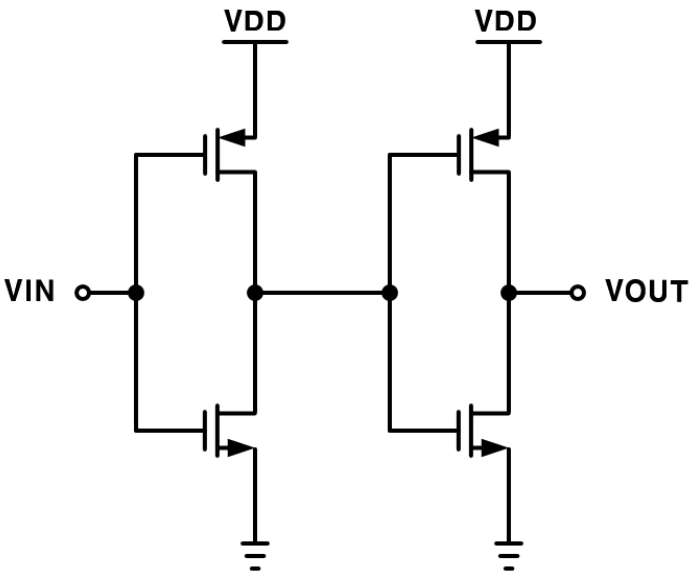

Figure 4.1. Threshold inverter quantizer

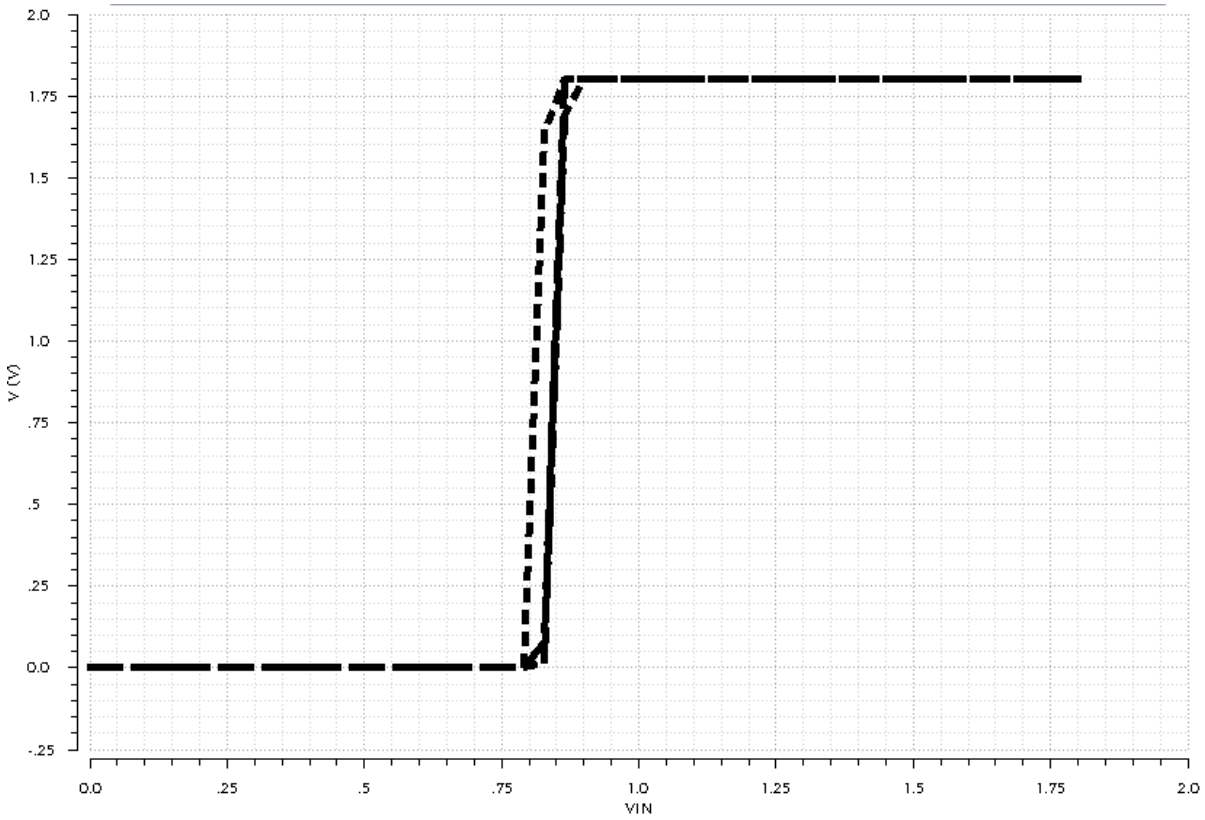

Figure 4.2. TIQ simulation result for temperature variation (-40℃, 27℃, 120℃)

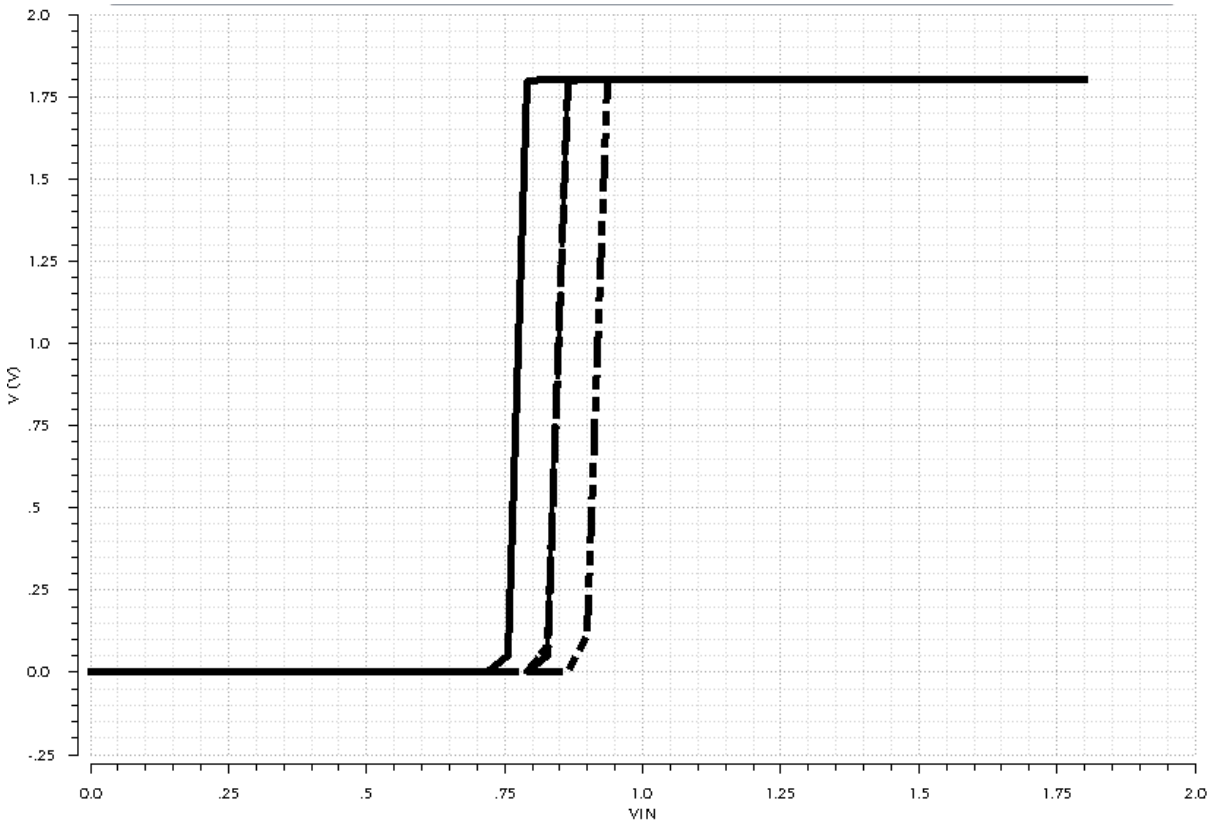

Figure 4.3. TIQ simulation result for process variation (TT, SS, FF, SF, FS)

V_{tn} and V_{tp} are the intrinsic threshold voltage of NMOS and PMOS. μ_p is the mobility of PMOS and μ_n is the mobility of NMOS. W_p and W_n are the width of both transistors. The threshold voltage of inverter is given the aspect ratio of W/L of NMOS and PMOS transistors. Usually when we design inverter, use same length of both transistors. Thus the value of the threshold voltage of inverter can be define W_n/W_n ratio.

The comparator was designed in 180nm TSMC process, the length is 20μm while using 220nm which is the minimum width for NMOS and 440nm for PMOS to minimize current consumption when the inverter is turned on. To do simulation VIN is changed from 0V to 1.8V which is V_{DD}. Figure 4.2 and Figure 4.3 are the simulation results of threshold inverter quantizer when the temperature and process are different. The temperature is used -40℃, 27℃ and 120℃. The process is used TT (Typical, Typical), SS (Slow, Slow), FF (Fast, Fast), SF (Slow, Fast) and FS (Fast, Slow). The drawback of this scheme is very weak from temperature and process variation. The threshold voltage is different depend on the circumstance. It is not reliable comparator so need to be designed very strong comparator which is independent of temperature variation and process variation.

4.2 Inverter based fully differential comparator with replica biasing

To do robust of temperature variation and process variation, add replica biasing circuit to inverter based comparator [14]. By using inverter based comparator, only when the input reach the vicinity of the threshold voltage the current flow. It can reduce current consumption. The left part of this comparator is for biasing circuit in Figure 4.4. Negative feedback is applied to fix biasing. Even though temperature and process are changed, the threshold voltage of the comparator follows V_{REF}.

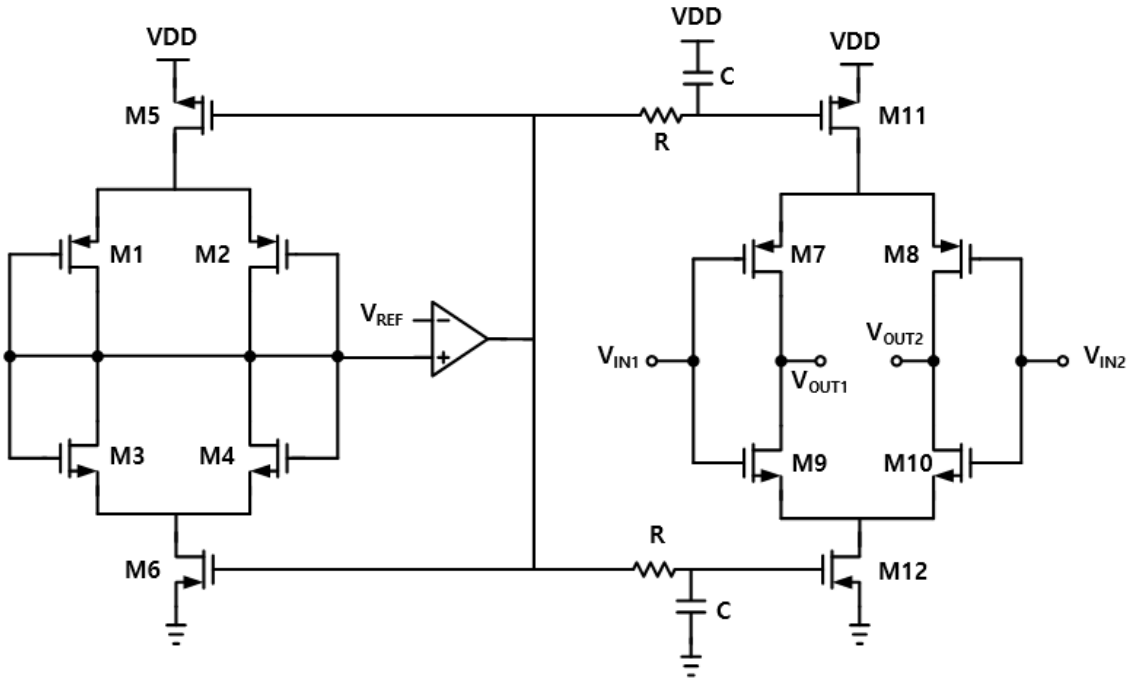

Figure 4.4. Inverter based differential comparator with replica biasing

I want to make reference voltage as VDD/2, so in this schematic V_{REF} is VDD/2. In the replica circuit there are PMOS current source and NMOS current source. To minimize current consumption, the length of PMOS and NMOS is used 20um and the width of NMOS and PMOS is 250nm and 500nm each. On the right side of the comparator, the width is 5 times larger than replica biasing circuit to improve speed. As a result the total current consumption is 1.4μA. Moreover, this comparator is very strong from temperature and process variation. (Figure 4.5 and Figure 4.6)

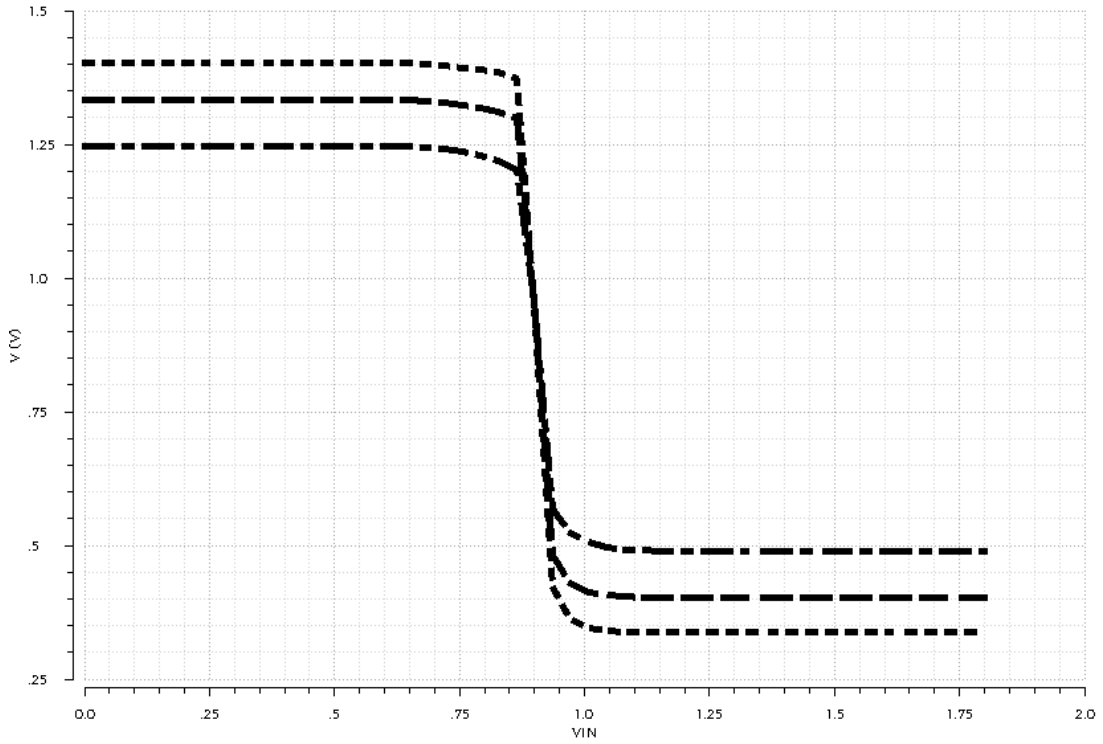

Figure 4.5. Simulation result of comparator with replica biasing for temperature variation

(-40℃, 27℃, 120℃)

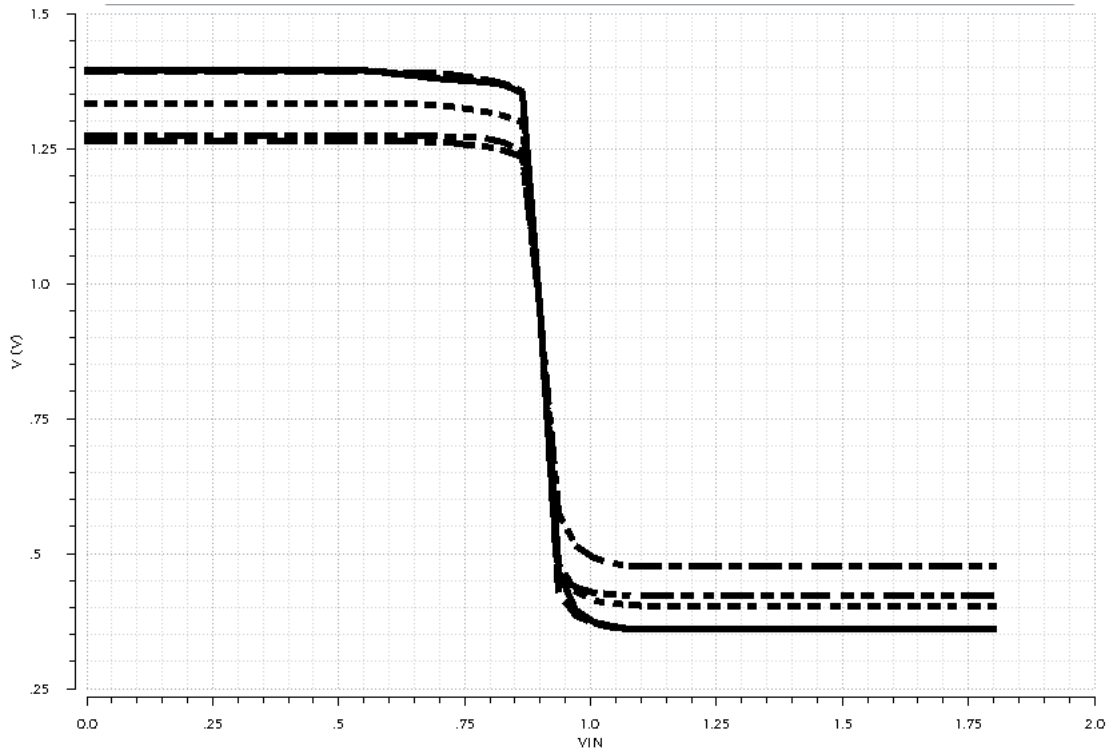

Figure 4.6. Simulation result of comparator with replica biasing for process variation

(TT, SS, FF, SF, FS)

VI. CONCLUSION

The wake up receiver is the assistant receiver to reduce the total power of receiver system. If there is no information from other transmitter, the main receiver is off. When the transmitter wants to transmit information, the transmitter sends a wake up signal and the wake up receiver detects it. In order to prepare to get the information, the main receiver is turned on by the wake up receiver. By additionally using the wake up receiver system to the main receiver system, the low power receiver system can be achieved. Moreover, by taking the advantage of fully differential topology, this baseband system is strong from the environment noise and coupling noise.

In this paper, envelope detector, programmable gain amplifier and comparator of whole baseband system for the wake up receiver are briefly explained. The envelope detector converts the high frequency signal around 2.4GHz to the baseband signal around 50kHz. Since the high frequency signal should go to the baseband signal without loss, the conversion gain is an important parameter. This envelope detector has a conversion gain as 1 when the input signal is 55mV. If the signal is less than 55mV, the conversion gain is also less than 1 and adversely the conversion gain is larger than 1, when the signal is higher than 55mV. It is profit in this system because one signal is smaller than 55mV and the other signal is over 55mV.

The output signal of envelope detector is amplified suitably by using programmable gain amplifier. The gain is 5V/V, 10V/V, 15V/V and 20V/V. The gain of programmable gain amplifier is defined the ratio of capacitor value by accompanying negative feedback network. It is robust from process, voltage and temperature (PVT) variation.

The replica biasing circuit is added to comparator. By using replica biasing technique, the threshold voltage of the comparator is fixed to the reference voltage which we usually use half

VDD. As a result, this comparator is also very strong from the temperature, voltage and process variation such as threshold voltage shift. By using inverter based comparator, only when the input reach the vicinity of the threshold voltage, the current flow. It can reduce current consumption.

TSMC 0.18nm process is used to design. The VDD is 1.8V and the total current consumption is around 20μm. In conclusion, the low power analog baseband system for the wake up receiver can be accomplished.

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요 약 문

Wake-Up 수신기를 위한 저전력 기저 대역 아날로그 회로 설계

Wake up receiver 는 정보의 수신이 없을 때에는 주 수신기를 꺼놓고 송신기에서 정보를 보낸다는 신호가 들어오면 wake up receiver 를 통해 신호 감지 후 주 수신기를 동작시키는 방식이다. 그 결과 정보의 송 수신이 없을 때에는 주 수신기가 동작하지 않아 불필요한 전력소모를 줄임으로써 저전력 구동이 가능하다. 나아가 fully differential 구조를 사용함으로써 환경 및 커플링 잡음에 강한 Wake up 수신기를 위한 기저 대역 아날로그 회로를 설계하였다.

본 논문에서는 wake up receiver 의 저주파 대역 시스템인 고주파 신호를 저주파 신호로 변환하는 envelope detector, envelope detector 의 출력을 원하는 만큼 조절하여 증폭이 가능한 programmable gain amplifier, 증폭된 신호를 최종적으로 0과 1로 결정하는 comparator 에 관한 연구를 수행하였다.

Envelope detector 는 common gate 구조를 사용하여 conversion gain 을 향상시키고, programmable gain amplifier 는 feedback 과 fully differential 구조를 사용하여 gain 을 capacitor 비율로 결정함으로써 외부 잡음으로부터 강하게 동작하도록 설계하였다. Comparator 는 replica biasing 회로를 추가하여 온도와 공정에 강인한 threshold voltage 을 갖도록 설계하였다.

TSMC 0.18㎛ 공정을 사용하여 1.8V 공급 전압에 약 14uA 전류 사용으로 동작하는 저전력 wake up 수신기 기저 대역 시스템을 완성하였다.

핵심어: Wake up 수신기, 기저 대역(Baseband), 포락선 검출기(Envelope detector), 증폭기(Programmable gain amplifier), 비교기(Comparator)