Master's Thesis
석사 학위논문

Development of Organic Floating-Gate Memory Transistors

Soyeon Jeon(전 소 연 田 素 涓)

Department of
Energy Science & Engineering

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Advisor: Professor Jongmin Choi
Co-advisor: Professor Jiwoong Yang

by

Soyeon Jeon
Department of Energy Science & Engineering
DGIST

A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Master of Science in the Department of Energy Science & Engineering. The study was conducted in accordance with Code of Research Ethics[1]

12. 18. 2020

Approved by

Professor Jongmin Choi (signature)
(Advisor)

Professor Jiwoong Yang (signature)
(Co-Advisor)

[1] Declaration of Ethical Conduct in Research**:** I, as a graduate student of DGIST, hereby declare that I have not committed any acts that may damage the credibility of my research. These include, but are not limited to: falsification, thesis written by someone else, distortion of research findings or plagiarism. I affirm that my thesis contains honest conclusions based on my own careful research under the guidance of my thesis advisor.

Development of Organic Floating-Gate Memory Transistors

Soyeon Jeon

Accepted in partial fulfillment of the requirements for the degree of Master of Science.

11. 23. 2020

Head of Committee Prof. Jongmin Choi (signature)

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ABSTRACT

Organic flash memories that employ solution-processed polymer semiconductors preferentially require internal stability of their active channel layers. In this paper, a series of new donor-acceptor copolymers based on cyclopentadithiophene (CDT) and diketopyrrolopyrrole (DPP) are synthesized to obtain high performance and operational stability of nonvolatile floating-gate memory transistors with various additional donor units including thiophene, thiophene-vinylene-thiophene (CDT-DPP-TVT), selenophene, and selenophene-vinylene-selenophene. Detailed analyses on the photophysical, two-dimensional grazing incident X-ray diffraction, and bias-stress stability are discussed, which reveal that the CDT-DPP-TVT exhibits excellent bias-stress stability over 10^5 s. To utilize the robust nature of CDT-DPP-TVT, floating-gate transistors are fabricated by embedding Au nanoparticles between Cytop™ layers as a charge storage site. The resulting memory devices reveal bi-stable current states with high on/off current ratio larger than 10^4 and each state can be distinguished for more than 1 year, indicating a long retention time. Moreover, a repetitive writing-reading-erasing-reading test clearly supports the reproducible memory operation with reversible and reliable electrical responses. All these results suggest that the internal stability of CDT-DPP-TVT makes this copolymer a promising material for application in reliable organic flash memory.

Keywords: Organic field-effect transistors, donor-acceptor copolymers, flash memory, high-performance, bias stability

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Ⅰ. Introduction

Polymer field-effect transistors (PFETs), in which polymer semiconductors with solution processability and mechanical flexibility are used as channel layers, have attracted significant attention as switching elements for flexible displays.[1-4] Thanks to tremendous research efforts in the last two decades, their electrical performances of charge carrier mobilities are comparable to those of hydrogenated a-Si FETs. These developments have enabled them to be applied in next-generation organic electronics such as organic image sensors and organic flash memories.[5-7] For example, the organic FET flash memories have received attention as core devices for realizing flexible electronic products. Vapor-deposited organic semiconductors, including pentacene and *N*,*N'*-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide, have thus far been extensively used as active layers in organic flash memories.[8-10] Thiophene-based conjugated polymer semiconductors such as poly(3-hexylthiophene-2,5-diyl) have also been often introduced to obtain PFET flash memories because solution-processed semiconductors have the clear advantages of large-area and low-cost production through inexpensive fabrication techniques; however, their low mobility and weak oxidative stability have hindered long-term uses of these memory devices.[11,12] In the meantime, newly designed polymer semiconductors exhibiting high electrical performances have been developed, for example, donor-acceptor (D-A) copolymer semiconductors.[2,13] The field of polymer semiconductors has advanced; therefore, an in-depth study is required to explore the feasibility of these D-A copolymer semiconductors being applied for organic FET flash memories.

As the flash memory generally controls a charge transfer between floating-gate and a semiconductor layer, it should overcome the morphological limitations of inherently polycrystalline or close-to-amorphous polymer semiconductors, which have inevitably resulted in bias stress instability, before they can be used for memory applications.[14,15] One known reason for such a bias instability of PFETs relates to charge trapping at the grain boundaries between crystalline domains within the semiconductor layer or dielectrics/semiconductor interfaces.[16-18] Therefore, when designing a new D-A copolymer semiconductor for the devices, both minimized interfacial trap states and a high carrier mobility should be considered to guarantee the operational stability within the thin films of the polymer semiconductor.

To quantitatively evaluate the bias-stress stability, the method of measuring the drain current under constant bias stress is also widely used with the following stretched-exponential time-dependent formula.[14]

$$I_D(t) = I_D(0)\left[-exp\left\{-\frac{t}{\tau}\right\}^{\beta}\right] \text{ when } |V_D| \ll |V_G| \quad (1)$$

I_D (0) is the initial drain current at $t = 0$. The values of τ, the mean time when charge carriers remain as mobile carriers, are typically compared to evaluate the bias stress instability of various PFETs. Several studies have reported the τ values of a variety of polymer semiconductors, which collectively reveal that τ is affected by the crystalline nature and adequate energy level of the polymer semiconductors. Regarding the crystallinity of the polymer semiconductors, for example, there is a general agreement that closer π-π stacking distances and interchain packing within the semiconductor thin films lead to higher bias stability.[19,20] These previous studies propose that careful molecular design of adequate energy levels and the crystalline nature can be a solution for PFET with high bias stability. Nonetheless, bias stability studies have been much less focused on recently developed high-mobility D-A copolymers than on small molecular semiconductors.

In this study, we newly synthesized four D-A copolymers with the aim of simultaneously realizing high performance and operational stability. These copolymers are based on cyclopentadithiophene (CDT) as a donor building block and diketopyrrolopyrrole (DPP) as an acceptor building block, with additional donor building blocks of thiophene (CDT-DPP-T), thiophene-vinylene-thiophene (CDT-DPP-TVT), selenophene (CDT-DPP-S), and selenophene-vinylene-selenophene (CDT-DPP-SVS). CDT is one of the most widely used electron donor units that are known to be beneficial for the long-range ordering of polymer microstructures. DPP is a strong acceptor unit, possessing a planar conjugated bicyclic lactam unit and thereby beneficial for interchain charge transport.[13,21] Based on the systematic analyses on the energetic and microstructural features of these new copolymers using ultraviolet-visible (UV-Vis) absorption spectroscopy and two-dimensional grazing incident X-ray diffraction (2D-GIXD), we found that the PFETs with CDT-DPP-TVT displayed negligible hysteresis and excellent bias stability with a τ of 5.33×10^5 s, making it the most fascinating candidate for application in electronic devices based on the transistor architecture. Finally, to fully utilize the advantage of the electrically reliable nature of CDT-DPP-TVT, we demonstrated a floating-gate memory transistor that utilized CDT-DPP-TVT as a channel layer, resulting in a robust memory operation.

Ⅱ. Experimental Section

2.1 Materials

All reagents and solvents were purchased from TCI Chemicals and Sigma-Aldrich, used without further purification.

2.2 Fabrication of OFETs and Memory Devices

A bare Si Highly n-doped Si^{++}/SiO_2 (100 nm) wafers were cleaned using piranha solution and oxygen plasma. After cleaning process, substrates were deposited with OTS, then annealed at 120 °C for 30 min. The solution concentrations of CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, or CDT-DPP-SVS are 5 mg mL^{-1} in chlorobenzene. Each polymer solution was spin-coated onto the OTS-treated substrate. These samples were annealed at 200 °C for 20 min in the N_2 filled glove box. Finally, the devices were completed by deposition of Au electrodes (80 nm) onto the active layer with a channel length of 150 and 1500 μm, respectively.

To fabricate the memory devices, Cytop™ solution was spin-coated onto the substrates and subsequently annealed at 200 °C for 1 hr. 2 nm thick Au layer was then thermally deposited using thermal evaporation to form Au NPs. After the deposition of Au NPs, the Cytop™ layer (7 nm) used as tunneling layer was deposited onto the Au NPs followed by annealing 200 °C for 1 hr. Thin film of CDT-DPP-TVT was deposited onto the Cytop™ layer by spin-coating a solution of polymer in chloroform. This sample was annealed at 200 °C for 20 min, and then 80 nm thick Au electrodes were deposited on the annealed films.

2.3 Thin Film and Device Characterization

UV-Vis absorption spectra were measured using an Agilent Technologies Cary 5000 spectrophotometer. 2D-GIXD measurements were conducted using PLS-II 3C and 9A beamline at the Pohang Accelerator Laboratory (PAL) in Korea. The morphologies of the Au NPs grown on Cytop™ layers were investigated using SEM (Hitachi, SU8230), and AFM (Park Systems, XE-150). The energy levels of the CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS thin films were characterized using UPS measurements (ESCALAB 250Xi) under ultrahigh vacuum ($<1 \times 10^{-8}$ torr), and an ultraviolet source of He I (21.2 eV) was used. The capacitance values of the dielectric layers were measured using Hewlett Packard 4284A LCR meter at 1 kHz. The capacitance of the OTS/SiO_2 layer, and dielectric layer (Cytop™/Au NPs/Cytop™/SiO_2) was 3.27×10^{-8} and 3.06×10^{-8} F cm^{-2}, respectively. The electrical characteristics of OFETs were measured in an N_2-filled glove box using

a Keithley 4200A-SCS.

Ⅲ. Results and Discussion

The synthetic route for preparing CDT-DPP-T, CDT-DPP-S, CDT-DPP-TVT, and CDT-DPP-SVS, whose chemical structures are shown in Figure 1a-d, are described in Schemes 1 and 2. The detailed synthesis procedures and analyses of the D-A copolymers are described in the Supporting Information.

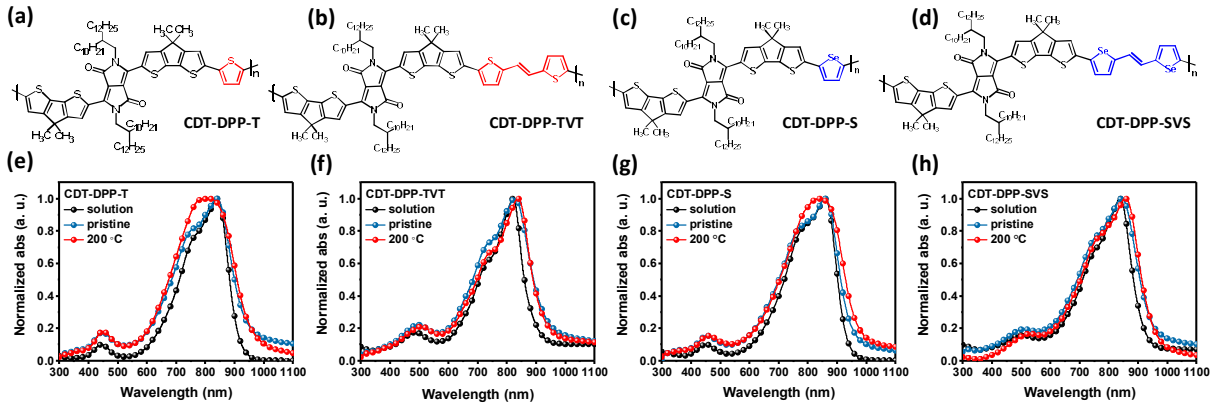

Figure 1. Molecular structures and normalized UV-Vis absorption spectra of (a, e) CDT-DPP-T, (b, f) CDT-DPP-TVT, (c, g) CDT-DPP-S and (d, h) CDT-DPP-SVS.

The optical properties and crystal aggregation behaviors of CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS were measured by using UV-Vis absorption spectra, as shown in Figure 1e-h. All polymers showed both band I and band II absorptions, which is a typical feature of D-A copolymers, and maximum absorption peaks are located near 850 and 450 nm, respectively.[23] Notably, the peaks of the absorption spectra were little red shifted from solution to solid states (thin films) in the all polymers, which implies that effective intermolecular π-π interactions were preferentially achieved in the solution states. However, in the cases of CDT-DPP-T and CDT-DPP-S, thermal annealing at 200 °C allowed these thin films to rearrange the polymer conformations, exhibiting increases in the intensity of shoulder peaks (0-1 vibrational peaks) relative to that of the 0-0 vibrational peaks.[22-24] On the other hand, the CDT-DPP-TVT, and CDT-DPP-SVS thin films showed similar absorption spectra even after the thermal annealing at 200 °C compared with their pristine forms. These different behaviors, depending on the thermal annealing, may result from the easy rotation of thiophene and

selenophene rings and different torsion configurations of the polymer chains.[23,25,26] Although the rearrangement of polymer conformations might induce efficient molecular packings to form more ordered crystalline structures, an easily changed structure depending on surrounding conditions such as temperature could affect the stability of the polymer thin films.[22,27,28] In this respect, CDT-DPP-TVT and CDT-DPP-SVS copolymers whose crystal aggregations are sufficiently formed in the solution state, may be more effective for stable operation by preventing internal instability of the semiconductor thin films when the device is driven.

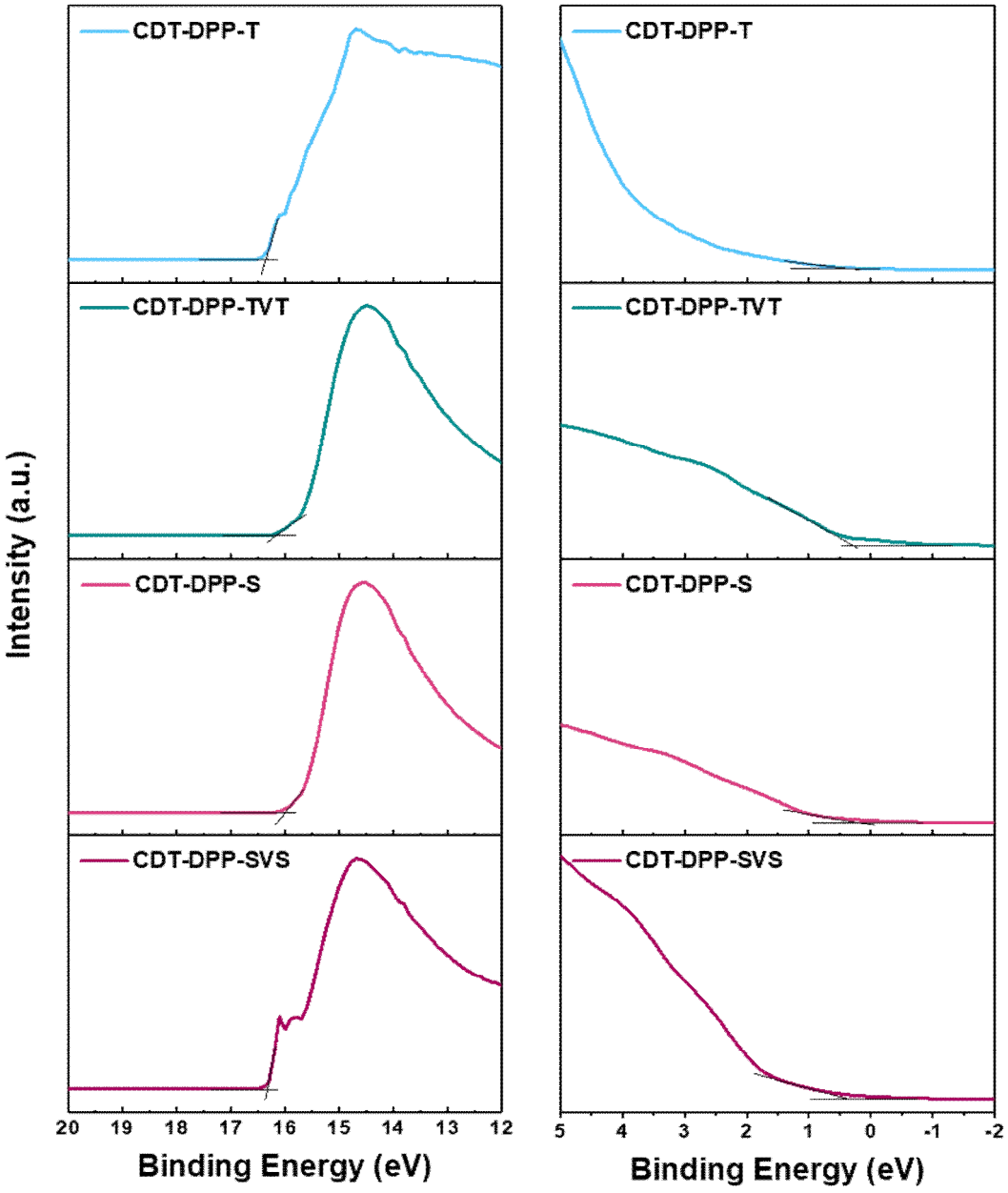

Figure S1. Ultraviolet photoelectron spectroscopy plots of the four polymers.

Table 1. Summary in optical and electrochemical properties of four different D-A copolymer semiconductors.

	UV-sol max (nm)	UV-Film max (nm)	UV-Film annealing max (nm)	UV-Film λ_{edge} (nm)	E_g (optical) (eV)	E_{HOMO} (eV)	E_{LUMO} (eV)
CDT-DPP-T	841	842	813	938	1.32	5.28	3.96
CDT-DPP-TVT	822	827	838	933	1.33	5.32	3.99
CDT-DPP-S	858	859	841	948	1.31	5.39	4.08
CDT-DPP-SVS	838	844	858	941	1.32	5.29	3.96

Molecular orbital energy levels were measured by ultraviolet photoemission spectroscopy (UPS) and UV-Vis absorption spectra. From the UPS spectra of all the polymer films, the ionization potential can be obtained from the secondary cutoff energy, as summarized in Figure S1. The obtained highest occupied molecular orbital (HOMO) levels are summarized in Table 1 together with other photophysical properties obtained from the UV-Vis absorption spectra. All the four polymers in this study possessed HOMO levels of 5.2–5.3 eV. The lowest unoccupied molecular orbital (LUMO) levels could be also calculated using the optical bandgaps of all the polymers measured using the UV-Vis absorption spectra: 1.32, 1.33, 1.31, and 1.32 eV for CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS, respectively (Table 1). From these results, we inferred that the energy levels of the four D-A copolymer thin films were little affected despite their different polymer conformations, torsion configurations, and conjugation lengths of the polymer chains.

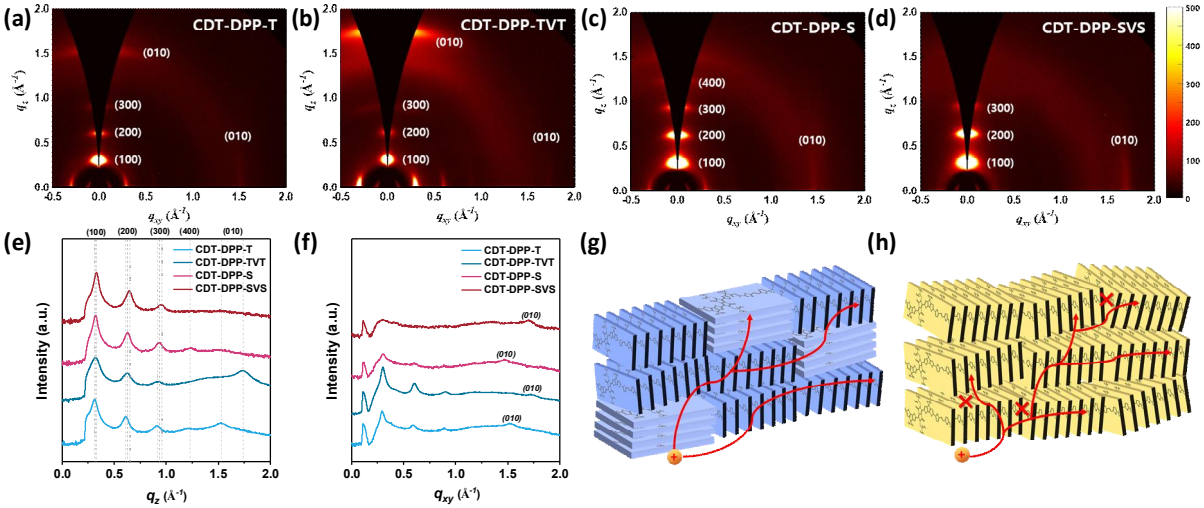

Figure 2. 2D-GIXD patterns of (a) CDT-DPP-T film, (b) CDT-DPP-TVT film, (c) CDT-DPP-S film, and (d) CDT-DPP-SVS film. (e) out-of-plane and (f) in-plane profiles extracted from 2D-GIXD images. (g) Schematic diagram of charge transport mechanism in three-dimensional orientations of CDT-DPP-TVT and (h) edge-on orientations of CDT-DPP-SVS.

Table 2. Summary in 2D-GIXD parameters of four different D-A copolymer semiconductors.

	π-π stacking distance (Å)	**d-spacing (Å)**	**g(010) (%)**	**g(100) (%)**
CDT-DPP-T	4.14	20.16	9.97	3.03
CDT-DPP-TVT	3.67	19.71	10.19	3.49
CDT-DPP-S	4.23	19.60	9.86	3.47
CDT-DPP-SVS	3.71	19.07	8.01	3.54

We conducted 2D-GIXD analysis to investigate crystal ordering in the D-A copolymer thin films using a high-resolution synchrotron X-ray beam source. Figures 2a-d compare the 2D-GIXD patterns of the CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS thin films, all of which were deposited onto the trichloro(octyl)silane (OTS)-treated SiO_2/Si substrates followed by thermal treatment. The intensity profiles along the out-of-plane (q_z) and in-plane (q_{xy}) were obtained from the 2D-GIXD patterns, as summarized in Figures 2e and f. The 2D-GIXD patterns revealed that all polymers typically adopted lamellar structures with Bragg patterns (l00) in the out-of-plane, implying that the four polymers had long-range ordering in crystalline structures. Based on the peak positions of (100) and (010), the d-spacing and π-π stacking distance of each lamellar structure of the D-A copolymers were estimated as summarized in Table 2. Both CDT-DPP-TVT and

CDT-DPP-SVS were found to represent short π-π stacking distances of 3.67 and 3.71 Å, respectively. These closer π-π stacking distances leads to large π-π overlap between adjacent molecular units, which contributes to favorable charge transport and reduces the generation of potential trapping sites.[19,29,30] In particular, (010) π–π stacking diffraction peaks appeared strongly in the out-of-plane direction for the CDT-DPP-TVT thin films and showed a (100) diffraction feature along with the in-plane direction, all implying that both edge-on and face-on orientation coexisted in the CDT-DPP-TVT thin films (Figure 2g, h).

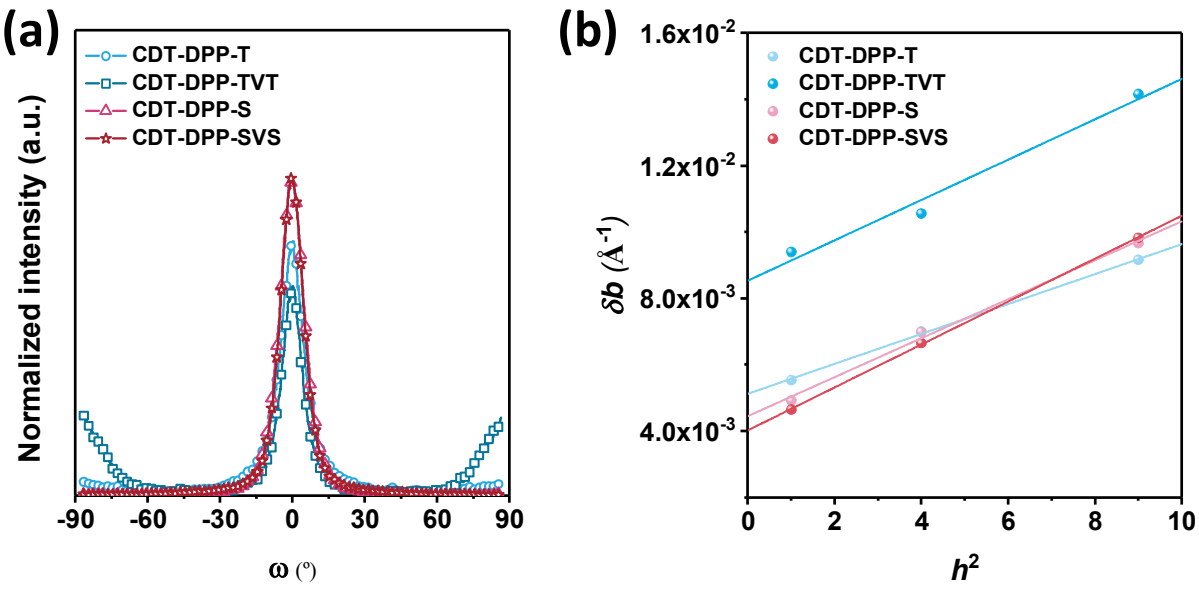

Figure S2. (a) The pole figures normalized by (200) scattered intensity and (b) δb-h^2 plots for CDT-DPP-T film and CDT-DPP-TVT film extracted from 2D-GIXD profiles in Figure 2.

To elucidate the orientation in the crystalline of the four polymers in detail, pole figure analysis was conducted based on (200) peaks in the out-of- plane direction to avoid using (100) scattering peak. The pole figure (Figure S2a) showed that CDT-DPP-S and CDT-DPP-SVS preferred the predominant edge-on packing structures compared to CDT-DPP-T and CDT-DPP-TVT. The 2D-GIXD, pole figure, and degree of crystalline perfectness (Figure S2b) imply that the CDT-DPP copolymers with thiophene and thiophene-vinylene-thiophene included crystals with three-dimensional orientations and coexisting edge-on and face-on orientations.[31-33]

The degree of crystalline perfectness was further analyzed quantitatively calculating the paracrystalline disorder. The paracrystalline disorder ($g_{(100)}$) in the out-of-plane (q_z) direction can be calculated from the δb–h^2 plot (Figure S2b) extracted from the 2D-GIXD patterns, where the slope (m) of the δb–h^2 plot is given by

$$m = \frac{g_{(100)}{}^2 \cdot \pi^2}{d} \quad (2)$$

where d is the domain spacing, δb is the integral widths of the diffraction peaks, and h is the order of diffraction. The paracrystalline disorder ($g_{(010)}$) of the polymer films for the in-plane (q_{xy}) direction can be also determined by

$$g_{(010)} = \sqrt{\frac{\Delta q}{2\pi q_0}} \quad (3)$$

where Δq is the width of diffraction peak, and q_0 is the center position of peck, respectively. As summarized in Table 2, the calculated $g_{(010)}$ values were 9.97, 10.19, 9.86, and 8.01 % for CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S and CDT-DPP-SVS film, respectively. Based on the microstructural analyses, CDT-DPP-TVT showed the smallest π-π stacking distances, and included a coexistence of the edge-on and face-on structures with more face-on dominant orientation.

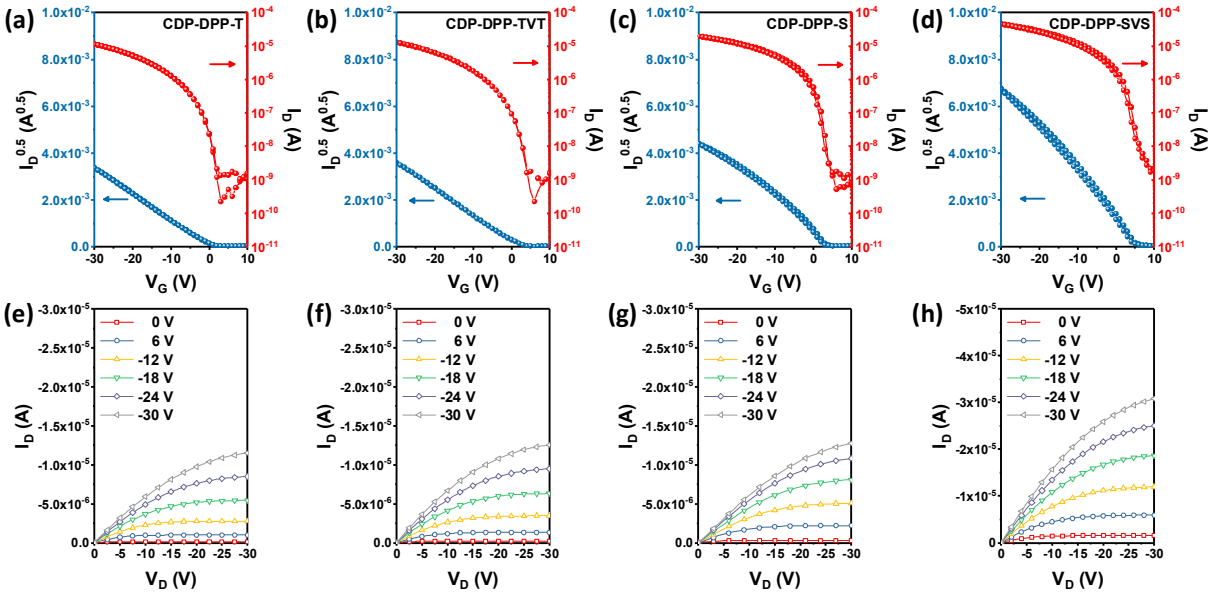

Figure 3. Transfer and output characteristics of PFETs with (a, e) CDT-DPP-T, (b, f) CDT-DPP-TVT, (c, g) CDT-DPP-S, and (d, h) CDT-DPP-SVS as active layers.

To investigate the effects of the microstructural features of CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS on their charge transport characteristics and internal instabilities, we fabricated bottom-gate top-contact PFETs using all the polymers as active semiconductor channel layers. The transfer and output characteristics of all polymers are summarized in Figure 3. The hole mobilities of the PFETs, measured from the saturation mode transfer characteristics, are shown in Table 3. It can be seen that the mobility values were higher

in the PFETs with edge-on dominant CDT-DPP-S and CDT-DPP-SVS than in the PFETs with CDT-DPP-T and CDT-DPP-TVT. However, the transfer characteristics of the PFETs with CDT-DPP-S and CDT-DPP-SVS thin films displayed double-slope characteristics in the square-root of drain current versus gate voltage ($I_D^{1/2}$-V_G) curves, which often occurs in some D-A copolymer PFETs.[34] This significant deviation from linearity originates from injection and trapping of minority carriers,[34,35] which would hamper the reliable operation when applying the PFET to flash memories. Given that all D-A copolymers spin-cast on the same substrates, such a kink in the transfer characteristics of PFETs is possibly related to the internal instabilities of the polymer semiconductors. In detail, charge carriers are vulnerable to trapping when injected into the channel because of a mismatch between the vertical flow of the carries from electrodes to a channel and the charge carrier transportation pathway in the edge-on orientation, which increases contact resistance between the semiconductor and electrode and thereby resulting in a kink in the $I_D^{1/2}$-V_G curves.[34,36] On the other hand, the PFETs with CDT-DPP-T and CDT-DPP-TVT thin films showed almost single-slope characteristics in the $I_D^{1/2}$-V_G curves without the kink effect. We infer that these D-A copolymers provide a three-dimensional charge carrier transportation pathway due to the coexistence of both edge-on and face-on orientation in the crystallites and reduce the carrier trapping and contact resistance (Figure 2g, h). Because the internal stability of active semiconductor channel layers should be guaranteed before their application in flash memories, we focused on CDT-DPP-T and CDT-DPP-TVT whose stabilities were demonstrated from the single-slope characteristics in the $I_D^{1/2}$-V_G curves and negligible hysteresis behavior in their transfer characteristics.

Table 3. Summary in electrical characteristics of the PFETs with four different D-A copolymer semiconductors.

	μ_{max} ($cm^2 V^{-1}s^{-1}$)	μ_{ave}[a] ($cm^2 V^{-1}s^{-1}$)	V_{th} (V)	I_{on}/I_{off}
CDT-DPP-T	0.13	0.11 ± 0.02	0.41 ± 0.03	10^4
CDT-DPP-TVT	0.15	0.13 ± 0.07	2.86 ± 0.03	10^4
CDT-DPP-S	0.19	0.17 ± 0.02	3.65 ± 0.05	10^4
CDT-DPP-SVS	0.22	0.20 ± 0.1	5.83 ± 0.1	10^4

[a] Mobility values were obtained from 32 independent devices for each PFETs.

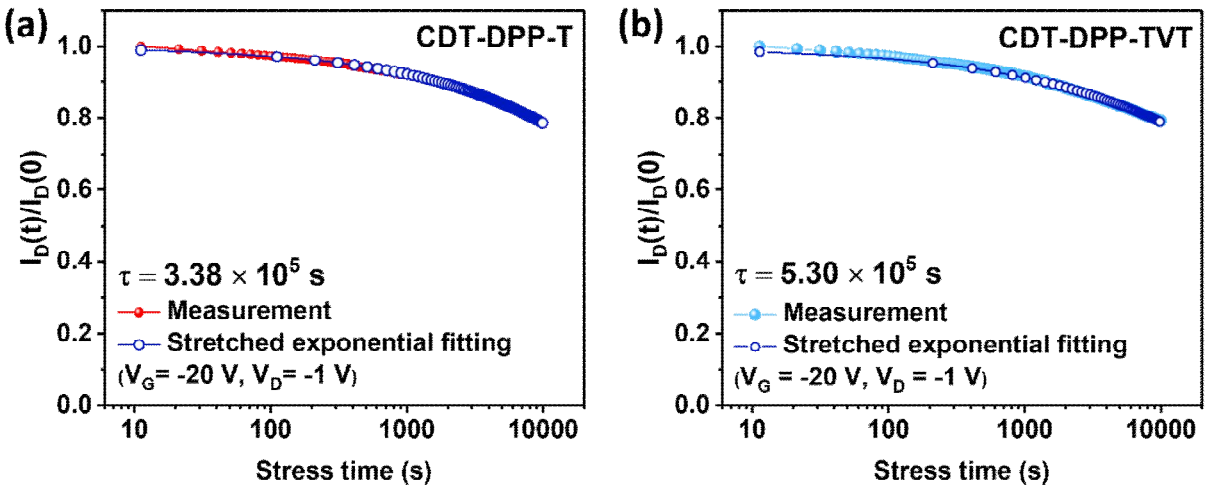

Figure 4. I_D decay plots of (a) CDT-DPP-T, and (b) CDT-DPP-TVT under gate bias-stress tests with an applied sustained bias of V_G = –20 V and V_D = –1 V.

Obtaining reliable operations of PFETs generally requires minimal charge trapping at the semiconductor-dielectric interfaces as well as within the semiconductor thin films. Therefore, we further investigated the bias-stress stability of the PFETs with CDT-DPP-T and CDT-DPP-TVT where Cytop™ layers were introduced to minimize semiconductor-dielectric interfacial trap states.[37] The bias-stress stabilities of these PFETs were characterized as shown in Figures 4a and b. We measured drain current (I_D) decay over a period of 10000 s under the applied voltage bias of V_G = –20 V and V_D = –1 V. After the bias stress for the given time, a decline in I_D for both devices with CDT-DPP-T and CDT-DPP-TVT was observed with the I_D decrease ratio of 22 and 19%, respectively. Values of τ and β for CDT-DPP-T and CDT-DPP-TVT obtained by fitting the I_D decay plots were 3.38×10^5 and 5.30×10^5 s and 0.41 and 0.50, respectively.[38] In other words, the PFET with CDT-DPP-TVT exhibited larger values of τ and β than that with CDT-DPP-T, indicating CDT-DPP-TVT showed significantly improved bias-stress stability compared to CDT-DPP-T. It may result from internal stability and decreased potential trap states of CDT-DPP-TVT, determined from the three-dimensional orientation of crystallites with short π-π stacking distances and large π-π overlap between adjacent molecular units. Therefore, we concluded that more a stable operation was obtained when reading the I_D of the PFET with CDT-DPP-TVT and the feasibility of applying CDT-DPP-TVT for floating-gate memory transistors is worth focusing on.

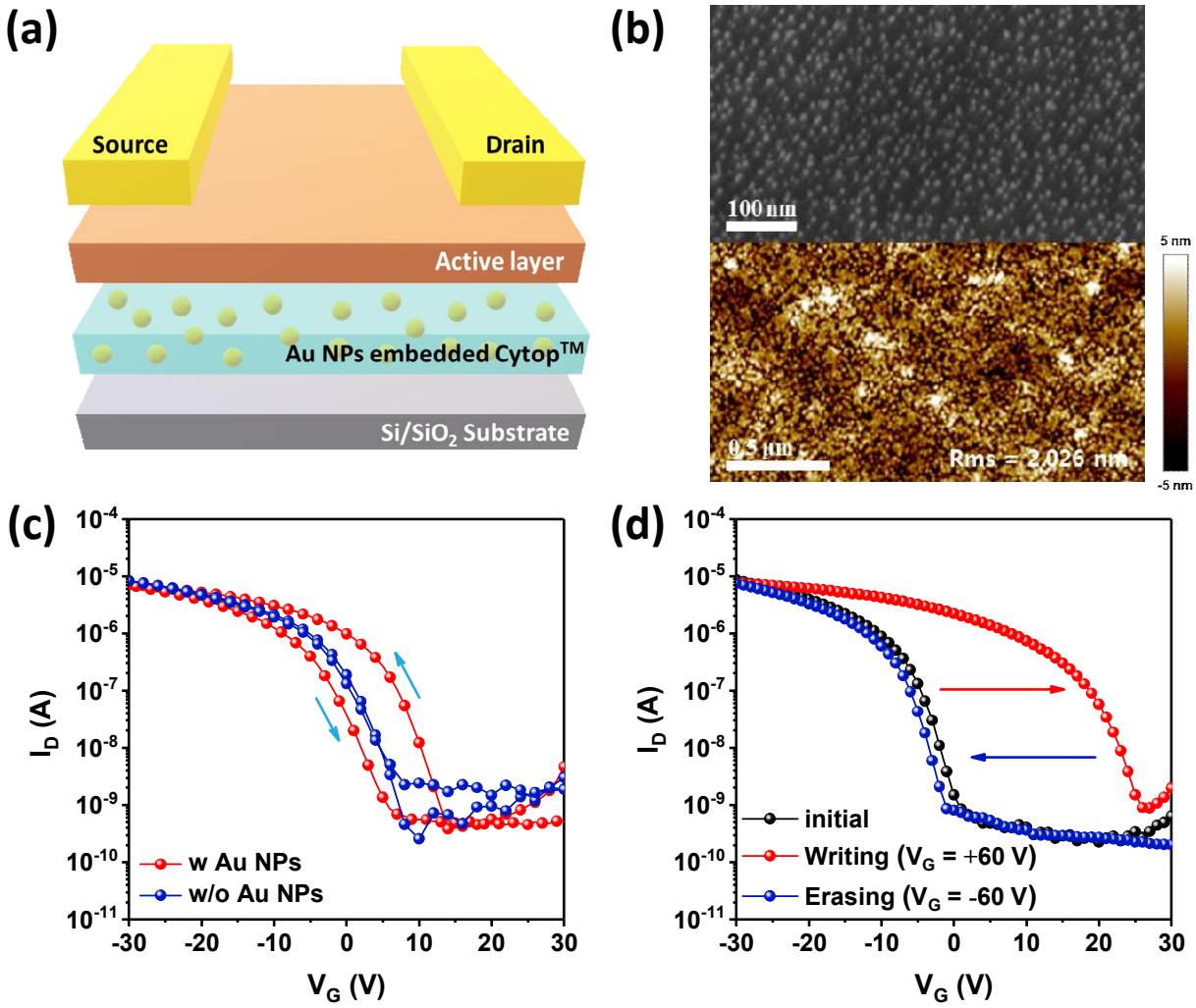

Figure 5. (a) Schematic device structure of the floating-gate memory transistor. (b) SEM and AFM images of Au NPs deposited onto the Cytop™ layer. (c) Transfer characteristics of the CDT-DPP-TVT PFETs with or without Au NPs. (d) Reversible shift in the transfer curves of floating-gate memory devices by applying V_G = +60 V and –60 V for writing and erasing processes, respectively.

To investigate the memory behavior of CDT-DPP-TVT, we fabricated a floating-gate memory transistor and measured its memory performances. Figure 5a shows the device structure of the floating-gate OFETs based on Au nanoparticles (Au NPs). Au NPs were introduced at the interface between the Cytop™ layers using a thermal evaporation process that is a conventional method in forming a charge storage site.[7,39] Figure 5b presents the scanning electron microscope (SEM) and atomic force microscopy (AFM) images of a 2 nm thick Au layer deposited on the Cytop™ layers.

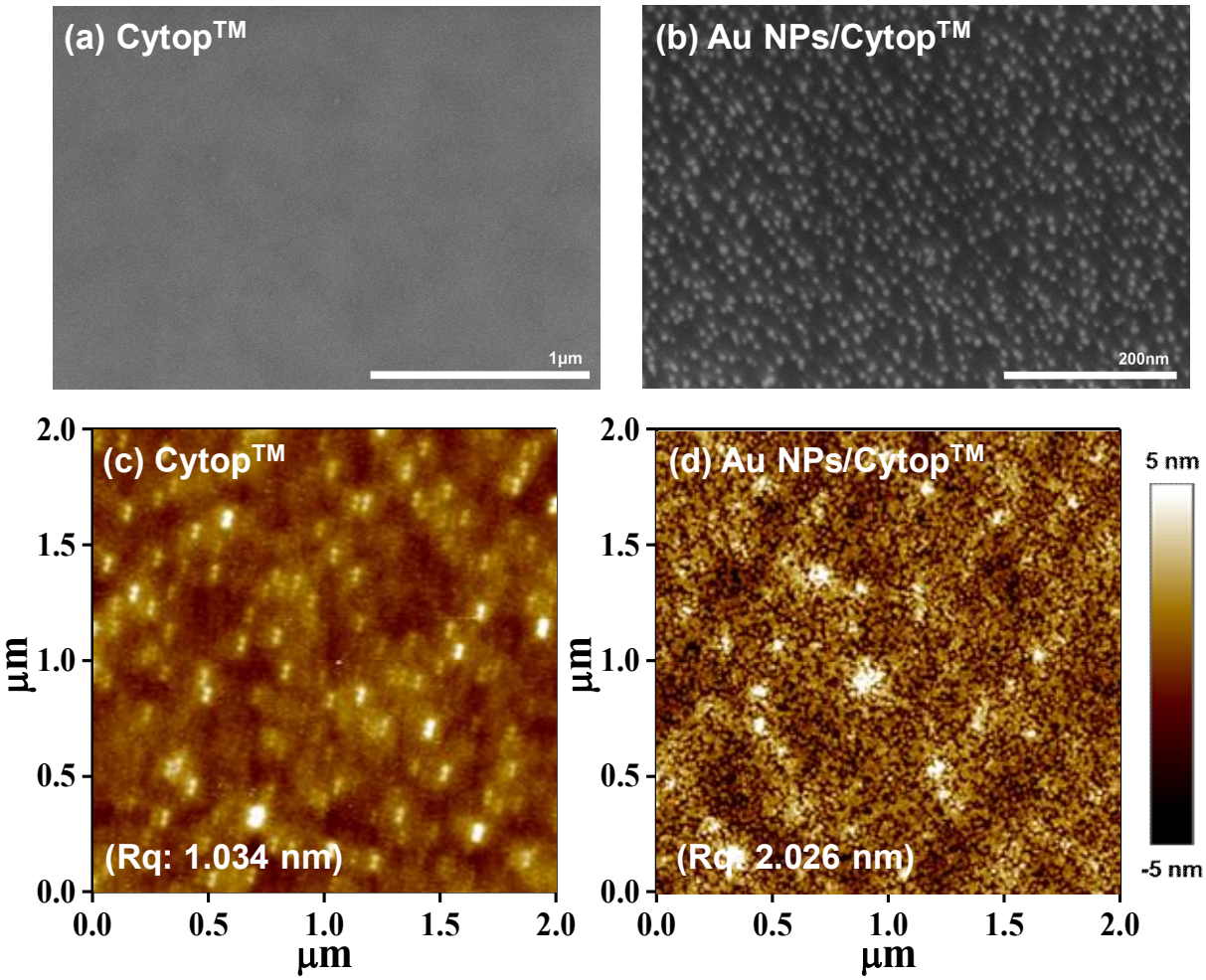

Figure S3. SEM and AFM images of (a, c) Cytop™ films and (b, d) Au NPs deposited onto Cytop™ layer.

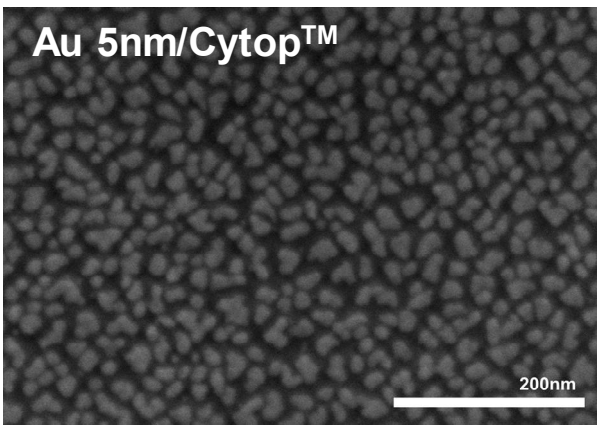

Figure S4. SEM image of 5 nm thick Au layer deposited onto Cytop™ layer.

Compared with the smooth surface of the Cytop™-coated sample (Figure S3a), each Au NP of size 10 nm can be observed to have isolated from other particles. The isolation of each Au NP should be required to block a

charge dissipation through the neighboring Au NPs in the flash memory application.[39,40] Thicker Au layer exhibited more aggregation of Au NPs compared to 2 nm thick Au layer (Figure S4). Therefore, a 2 nm thick Au layer was considered as an optimized condition for the fabrication of the PFET memory with CDT-DPP-TVT. Figure 5c represents the transfer characteristics of the CDT-DPP-TVT PFETs with or without the Au NP layer. The PFETs without Au NPs showed negligible hysteresis during gate voltage (V_G) sweep, whereas the device with introduced Au NPs as a floating gate layer displayed observable hysteresis during the V_G sweep ranging from –30 to +30 V. This result indicated that embedding Au NPs between Cytop™ layers acted as charge trap site and allowed the device to display a memory window, defined as the V_{th} difference between the writing and erasing processes. These memory windows are related to the hysteresis behavior in the transfer characteristics.[39,41] As shown in Figure 5d, we measured the transfer characteristic of the floating-gate memory transistor using electron trapping mode, because it is important to read out the memory states at 0 V of gate bias and obtain distinct two ON and OFF current states for long-time usage.[42-44] Threshold voltage (V_{th}) shifts were generated by applying a gate bias of V_G = ±60 V for 1 s. After application of a positive gate bias of V_G = +60 V for 1 s, defined as a writing process, a positive shift was observed with a V_{th} shift at approximately 25 V. This V_{th} shift was attributed to the electron trapping where the negative charges stored in the Au NPs facilitate accumulation of hole channels despite at the positive V_G.[39,41] Therefore, this writing process allowed an on-state saturation current obtained at V_G = 0 V. On the other hand, the transfer curves shifted to the negative direction by applying a negative gate bias of V_G = –60 V, defined as an erasing process, with a V_{th} shift of 28 V. The erasing curves recovered to the initial state, and this result revealed that tunneling of the trapped charges in the Au NPs easily transferred to the channel layer.[41,45] The trapped charge density (Δn) in Au NPs was calculated by the following equation:

$$\Delta n = \frac{C_i \Delta V_{th}}{e} \quad (4)$$

where, C_i is the capacitance of dielectric layer (3.06×10^{-8} F cm^{-2}), ΔV_{th} is the threshold voltage, and e is the charge of an electron. From this equation, we calculated charge trap density of Au NPs to be 4.78×10^{12} cm^{-2}. The number of Au NPs was determined from SEM image as shown in Figure S3b and, ~2182 Au NPs were present within a 2.76×10^{-9} cm^2 area. Therefore, we concluded that approximately ~1.26 electrons were trapped in one Au NP and this result is similar to reported paper.[39] We could obtain reproducible writing and easing characteristics of memory devices with CDT-DPP-TVT by applying a gate bias. The memory window was different from the magnitude of gate bias, as summarized in Figure 6a. The positive shifts of the transfer curves

and corresponding memory window (Figure 6b) increased as the magnitude of the gate bias increased, suggesting that stored charge density in Au NPs is proportional to the applied bias and induced memory window.[43,46]

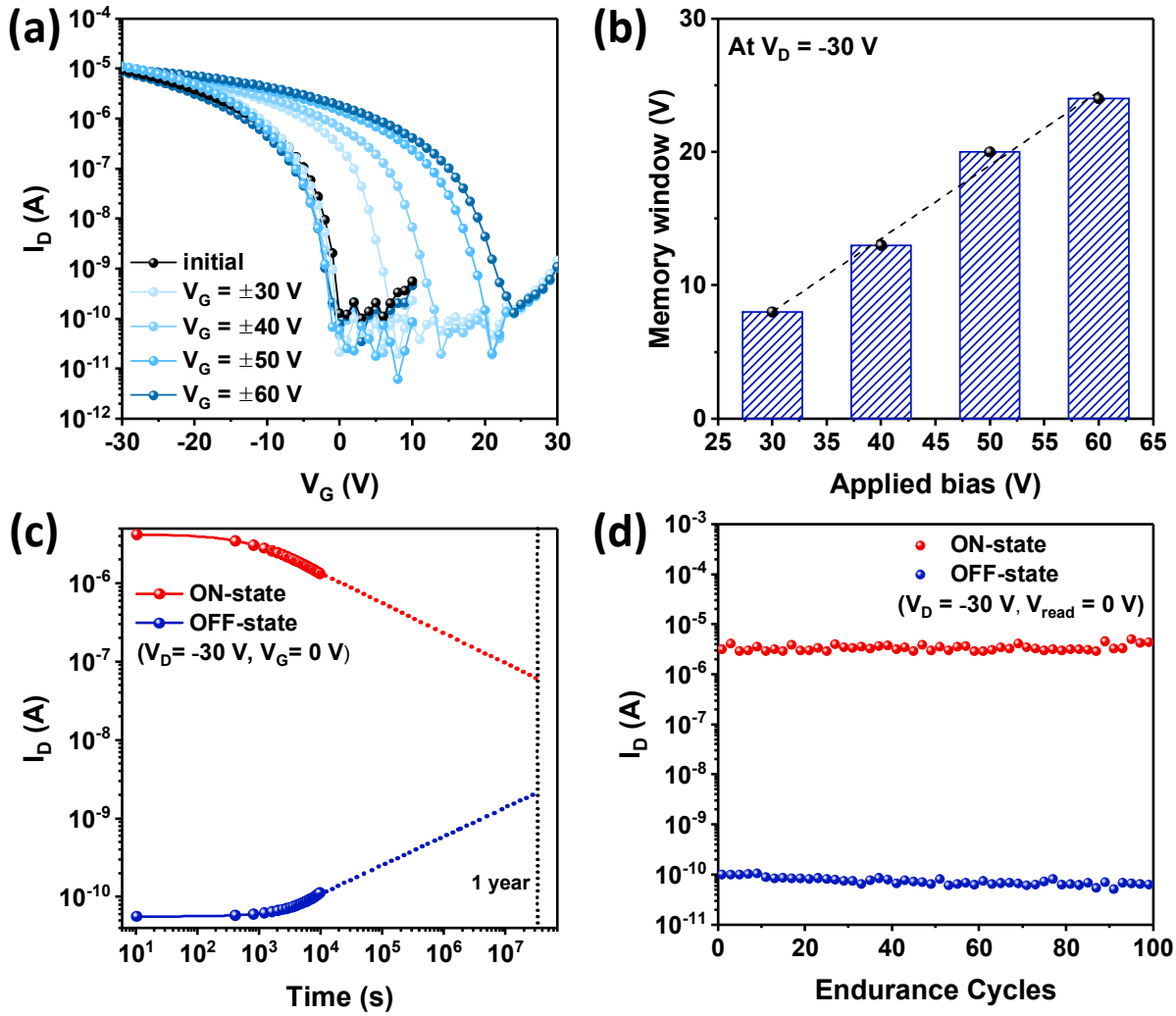

Figure 6. (a) V_{th} shifts in the transfer curves of the CDT-DPP-TVT memory device with various magnitudes of gate biases. (b) Comparison of memory windows by application of different gate biases. (c) Retention characteristics of memory device measured at a V_G of 0 V and V_D of –30 V. (d) Reversible WRER cycles of the floating-gate memory device.

The positive shifted transfer curves after the writing process under an applied V_G of +60 V for 1 s enabled us to obtain an on-state saturation current at a V_G of 0 V, resulting in ON state of memory devices. After V_{th} shifted to initial state by the erasing process when a negative bias (V_G = –60 V for 1 s) was applied, a current below 10^{-10} A was obtained at V_G = 0 V, meaning that OFF state of memory devices. As shown in Figure 6c, the ON and OFF bi-stable current states were found to be maintained over 10000 s. The extrapolation implies that

each state can be distinguished for more than one year.[41] These results demonstrated that the device with a CDT-DPP-TVT active channel operated stably while the Au NPs system had distinct property in charge storage. Figure 6d illustrates the dynamic switching behavior of floating-gate memory with CDT-DPP-TVT. The reversible current response of the switching behavior was tested by writing-reading-erasing-reading (WRER) cycles. V_G of writing, reading, and erasing was +60V (1 s), 0 V, and –60 V (1 s), respectively. The writing/erasing processes changed the ON/OFF current states significantly over 100 cycles, displaying a good reversibility and stability of the memory device. These results showed that excellent reliability of organic memory devices was realized using the CDT-DPP-TVT thin film, which has robust internal stability.

Ⅳ. Conclusion

We designed four novel D-A copolymers with different donor building blocks: CDT-DPP-T, CDT-DPP-TVT, CDT-DPP-S, and CDT-DPP-SVS, and studied their feasibility as semiconductor channel layers for high-performance floating-gate memory transistors. Each copolymer induced different molecular arrangements that affected crystal aggregation behaviors and intermolecular π-π interactions in its thin film. The 2D-GIXD analysis revealed that the CDT-DPP-TVT showed coexistence of edge-on and face-on orientations and short π-π stacking distances with large π-π overlap between adjacent molecules, contributed to internal stability. We consequently found that the PFETs with CDT-DPP-TVT showed negligible hysteresis and excellent bias-stress stability compared with other polymers. Utilizing the CDT-DPP-TVT thin film, nonvolatile memory behaviors were investigated by fabricating floating-gate memory transistors with Au NPs as a charge storage layer. These memory devices precisely responded to (+) and (–) gate biases and showed a maximum memory window of 28 V. As a result, the ON and OFF bi-stable current states were clearly obtained, and these states could be distinguished over 1 year after one writing and erasing process. These memories also exhibited reproducible switching operations during 100 repetitive WRER cycles. Our study demonstrated that designing CDT based D-A copolymers can be an effective strategy to guarantee the operational stability within the semiconductor channel layers and to satisfy the requirements of reliable organic memory transistor applications.

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요 약 문

유기 반도체를 이용한 플로팅 게이트 메모리 트랜지스터 개발

본 논문은 유기 반도체를 이용한 플로팅 게이트 메모리 트랜지스터 개발 방법을 제시한다. 용액공정을 이용한 유기 플래쉬 메모리는 활성층의 내부 안정성이 중요하다. 높은 성능과 안정성의 비휘발성 플로팅 게이트 메모리 트랜지스터를 구현하기 위해 사이클로펜타디티오펜 (cyclopentadithiophene, CDT) 및 디케토피롤로피롤 (diketopyrrolopyrrole, DPP)에 기반하여 티오펜(thiophene), 티오펜-비닐렌-티오펜 (thiophene-vinylene-thiophene, TVT), 셀레노펜 (selenophene), 그리고 셀레노펜-비닐렌-셀레노펜(seleno-phene-vinylene-selenophene, SVS) 등 다양한 전자 주개-전자 받개 공중합체가 합성되었다.

위 4가지 전자 주개-전자 받개 공중합체를 바탕으로 광물리학적, 2차원 스침각 X-선 회절 분석법 및 바이어스 안정성에 대한 상세한 분석이 논의된다. 특히 바이어스 안정성 분석에서 CDT-DPP-TVT는 stress time이 10^5초를 넘는 우수한 안정성을 보여주었으며, 이러한 CDT-DPP-TVT의 특성을 활용하기 위해 전하 저장 장소로 금 나노 입자를 사용하여 플로팅 게이트 메모리 트랜지스터를 제조하였다. 결과적으로 메모리 트랜지스터는 10^4 보다 높은 on/off 전류 비율과 on과 off 상태에서 각각 1년 이상의 긴 보유시간을 나타냈다. 또한 반복적인 쓰기-읽기-지우기-읽기 평가를 통해 가역적이고 안정적인 메모리 트랜지스터 구동이 가능함을 보여주었다. 이러한 결과는 높은 내부 안정성을 지닌 CDT-DPP-TVT와 같은 공중합체가 신뢰성 있는 유기 플래쉬 메모리의 소재로써 유망한 재료임을 시사한다.

핵심어: 유기 전계 효과 트랜지스터, 전자 주개-전자 받개 공중합체, 플로팅 게이트, 플래쉬 메모리, 바이어스 안정성