Master's Thesis
석사 학위논문

High Input Impedance OTA-Less NS-ADC with Chopped VCO for Multi-channel, Non-invasive EMG Monitoring

Yoonsung Choi(최 윤 성 崔 允 誠)

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Co-advisor: Professor Hongki Kang

by

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A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Master of Science in the Department of Information and Communication Engineering. The study was conducted in accordance with Code of Research Ethics[1]

. . 2020

Approved by

Professor Junghyup Lee (signature)
(Advisor)

Professor Hongki Kang (signature)
(Co-Advisor)

[1] Declaration of Ethical Conduct in Research**:** I, as a graduate student of DGIST, hereby declare that I have not committed any acts that may damage the credibility of my research. These include, but are not limited to: falsification, thesis written by someone else, distortion of research findings or plagiarism. I affirm that my thesis contains honest conclusions based on my own careful research under the guidance of my thesis advisor.

High Input Impedance OTA-Less NS-ADC with Chopped VCO for Multi-channel, Non-invasive EMG Monitoring

Yoonsung Choi

Accepted in partial fulfillment of the requirements for the degree of Master of Science.

. . 2020

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ABSTRACT

Power, area, and input impedance are important parameters for multi-channel, non-invasive EMG monitoring. In addition, 1/f noise and 3rd harmonic due to nonlinearity must be considered. Recently, while dealing with the above problems, a VCO-based ADC has been high-lighted. VCO based ADC improved the efficiency by making the circuit digital-intensively. However, it still has 1/f noise, input impedance, and area issues.

This paper focuses on solving the above problems in the simplest way. Chopping is applied directly to the VCO to eliminate 1/f noise. However, as a disadvantage, noise is generated every certain period, which degrades the noise performance of the entire structure. Total input capacitance (only bulk of the VCO is seen) are reduced by using DC-coupled input. Therefore, the input impedance is obtained to 1Gohm. The ADC structure based on open circuit obviates to consider DAC complexity. The elimination of the analog block further lowers power consumptions. Thus, the area occupies 0.028mm2 and ADC consumes 2uW. Also, by using bulk-driven VCO, we achieved 72dB of SFDR performance without any additional technique.

Keywords: Multi-channel, Non-invasive, EMG, Input Impedance, VCO-based ADC

List of Contents

List of tables

List of figures

1. INTRODUCTION

1.1 Area of Focus

With the growing demand to care for one's health condition in real-time, the need for miniaturized sensors has been studied in the recent few decades. Still, there are demands for the sensor with higher performance. Particularly, the power and area efficiency are the key focuses for a multi-channel sensor. Additionally, a non-invasive electrode also requires a large input impedance condition.

1.2 Background of Direct ADC

The methodology for measuring bio-signals can be categorized into two ways [1-4]. 1) High gain amplifier (IA) + low-resolution ADC 2) Direct ADC. A conceptual block diagram is introduced in figure 1.

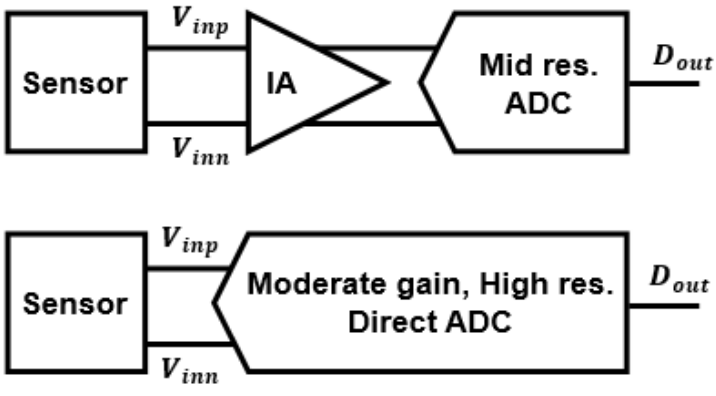

Figure. 1.1. Conceptual block diagram of the conventional IA + ADC architecture (top) and direct digitizing architecture with a sensor front-end embedded ADC (bottom).

The IA + ADC method is the structure that has been used in the earliest days. It is a structure that can reduce ADC design complexity and required performance cost by arranging an IA with a large gain of about 80dB. The problem with this structure is that the dynamic range of the input signal cannot be greatly increased due to the high gain of IA. The above problem is a particularly crucial defect in bio-applications because of the presence of relatively large artifacts. Although a lot of efforts were made to develop IA [5-8], the use of the IA+ADC structure is limited to applications with a small input signal range. The performance is still degraded by large inputs and the structure of the IA becomes complicated to endure large inputs.

Direct ADC came out to solve the problem caused by the high amp gain and large artifacts. Direct ADC structure uses amp with moderate gain and high-resolution ADC. In general, the Delta-sigma modulation (DSM) structure is widely used for ADC [9-11]. By using this structure, it was possible to take a large DR and reduce the overall complexity required by the architecture. However, as the burden of the ADC increases, the power and area consumed by the ADC increase. Besides, since it has an analog-based structure, it does not take advantage of increasing technology scaling.

Existing direct ADCs were mostly modified versions of continuous-time DSM (CT-DSM) structure. Figure 2 shows the conventional capacitively coupled CT-DSM. This structure has improved noise performance, better linearity due to loop gain, and more accurate gain accuracy. However, the problem with this structure is 1) Since voltage-domain loop filters still operate in the analog domain, cannot take a low supply voltage when considering

noise performance, input swing, and linearity. Thus, power consumption is limited. 2) As it uses the chopping technique, it has a lower input impedance while using a larger input cap.

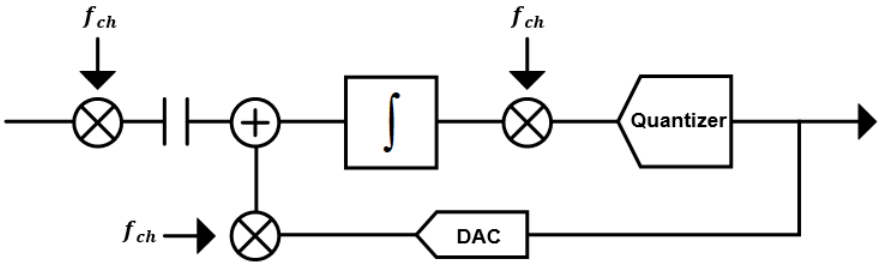

Figure. 1.2. conventional capacitively coupled CT-DSM Structure

1.3 Background of VCO-based Direct ADC

Recently, processing information in the phase domain rather than the voltage domain has been introduced. [12-15]. Among them, using a voltage-controlled ring oscillator (VCO) as an integrator and quantizing information in the phase domain is highlighted. The aforementioned VCO-based ADC has a few advantages. Multi-stage VCO naturally provides multi-level quantization and DAC element matching (DEM) ability. Due to the digital intensive nature, it can also benefit from technology scaling. For the above reasons, VCO-based ADCs show the possibility to expect better performance.

As shown in Figure 3, VCO-based ADC can be divided into two ways. 1) frequency domain quantization 2) phase domain quantization.

In frequency domain quantization in the figure. 3 (a), the input voltage is changed into frequency information via VCO. VCO output edges are detected by using XOR-DFF blocks or

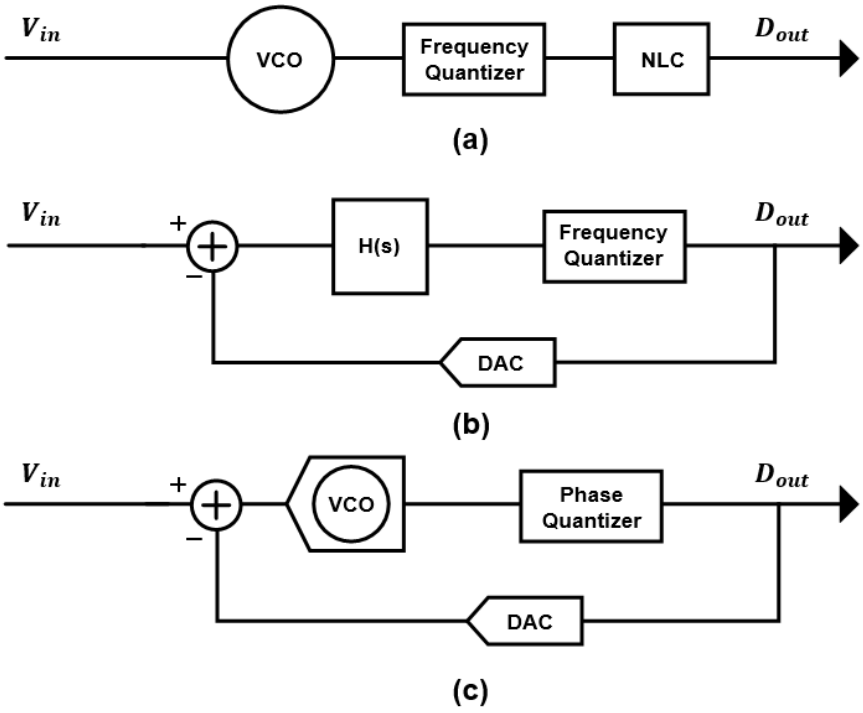

Figure. 1.3. Block diagram of two approaches of VCO-based ADC. (a) Frequency-based quantization.

(b) Frequency-based quantization with closed loop system (c) Phase-based quantization

counters. Then, input voltages and frequency domain digital outputs have linear relationships so that complete frequency domain DSM operation. A representative example is in this paper [16]. This structure has no OTA. VCO replaces OTA and plays a role as an integrator. Since the non-linearity of VCO degrades overall SFDR performance, a complex non-linearity correction (NLC) was used to obtain a 79dB spurious-free DR (SFDR) for 100-mVpp input swing.

Another way to solve the non-linearity problem is shown in figure 3 (b). To solve the non-linearity problem, placing VCO into a closed-loop system with an analog loop filter H(s). The non-linearity of VCO is suppressed by the gain of H(s). Moreover, this structure has an

intrinsic DEM capability. Due to the differentiated VCO's digital output, the DAC elements are naturally chosen in a barrel shifted fashion. As a result, DAC mismatch is automatically first-order noise shaping. [17] However, the problem of this structure is that H(s), an analog part, consumes large power, occupies a large area, and unfriendly with technology scaling. In particular, the XOR-DFF based structure eliminates the integration capability of the VCO. Equation (1) shows a gain from VCO to frequency quantizer. Voltage to frequency gain of VCO, k_{vco}, is relatively large but sampling frequency fs is also high. Gain from VCO to digital output cannot provide enough loop gain. Thus, VCO input experiences a relatively large input swing, which degrades SFDR performance.

$$Gain = \frac{k_{vco}}{s} \cdot st_s. \tag{1}$$

Therefore, the input of the VCO still sees a large signal swing and limits the overall ADC linearity performance. To address this problem, [18] uses phase information instead of frequency information (see Figure 2.3 (c)). Since there is no differentiation in the loop, the VCO operates as an integrator and improves the loop gain. Also, this structure uses a dual VCO scheme, so that the center frequency of the VCO can be determined irrespective of the sampling frequency, and thus the power of the VCO and the performance of phase noise can be improved [19]. In terms of the overall linearity of the ADC, the analog loop filter H(s) is no longer needed thanks to the large gain of the VCO and multi-stage. However, it still has more challenges to solve, such as 1/f noise and input impedance problems.

1.4 Preview Proposed ADC

In this paper, we present an open-loop VCO-based ADC for multi-channel EMG acquisition. It is the simplest direct ADC using an only chopper, VCO, and counter, it has the following advantages.

1) By directly applying the chopping technique to the VCO, 1/f noise is removed. DC-coupled input makes input impedance high. Also, by removing OTA or any other analog blocks, it brings low supply voltage and consequently reduces power consumption and area.

2) Thanks to body-biased VCO, VCO-based ADC achieved 72dB SFDR without any additional technique.

3) Open-loop structure using VCO and counter as a quantizer helps to achieve high input DR. Furthermore, stability and DAC cost are no more concerns.

The prototype chip was manufactured in the 180nm process, occupies an area of 0.028mm^2, obtained 64.6 SNDR and 72dB SFDR with a 70mVpp input range. IRN performance is 22uVrms with 200Hz BW, 2uW power consumption, and an input impedance of 0.7G ohm.

1.5 Thesis Overview

This paper is organized as follows. Section II describes the architecture of the proposed VCO-based ADC using a chopping technique directly to the VCO and also each block is discussed. Section III presents the measurement results and comparison. The conclusion

is drawn in Section IV.

2. Proposed OTA-Less NS-ADC with Chopped VCO

2.1 Overview of Proposed system

We introduce a VCO-based ADC for multi-channel EMG signal acquisition. Proposed VCO-based ADC obtaining high input impedance, low power, and low area while having the simplest structure. Fig 2.1. shows the conceptual block diagram of proposed ADC.

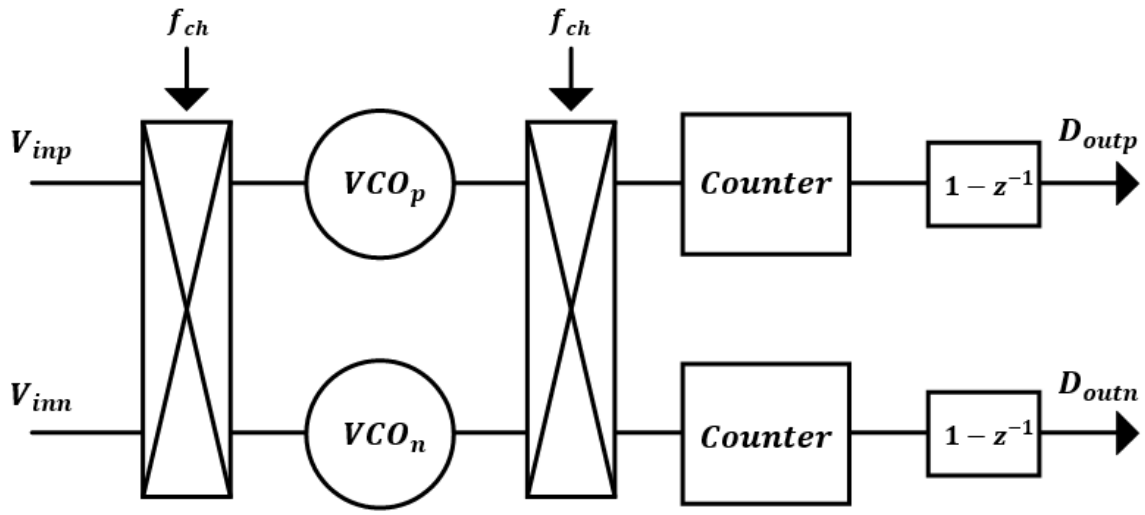

Figure. 2.1. Conceptual block diagram of proposed ADC

3-stage ring VCO acts as a loop filter for the entire ADC structure. The input signal is chopped before connected to VCO block. VCO integrates the input voltage to the phase domain. Then, integrated phase domain information is chopped again, and the signal comes back to in-band. Simultaneously, the 1/f noise of VCO modulated to out-of-band and eliminated. the final digital output is achieved through a counter and differentiator. A

signal diagram is shown in the figure. 2.2. Overall loop gain is derived as $k_{vco} \cdot t_s$, where, k_{vco} is the tuning gain of the VCO and t_s is the sampling time. Quantization error, Q_e, is 1st order noise-shaped. $Q_{fch,error}$ represent flat noise caused by the chopping technique. This error will be explained later.

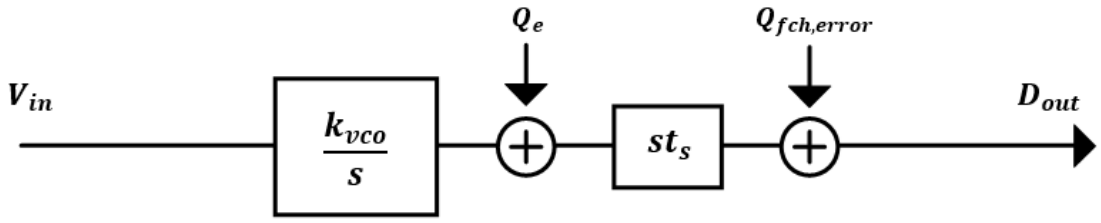

Figure. 2.2. Signal diagram of the proposed system

2.2 Direct chopped VCO

2.2.1 Behavior of Chopped VCO

The proposed direct chopped VCO, two VCOs' phase output is chopped differentially. That is, VCOs have each other's phase complementary at every chopping frequency. Table. 1 and Table. 2 explain the VCO behavior scenarios respectively. Note that the proposed architecture chooses DC-coupled input to have higher input impedance. DC-coupled sees only parasitic capacitances related to VCO body gate. In contrast, AC-coupled total input capacitance reaches a range of several pf. Larger input capacitance further lowers the input impedance, $Z_{in} = 1/fc$. Therefore, the input impedance is limited in the range of tens of Mohm.

The phase integration of conventional VCO is briefly reviewed. The input is integrated into

the phase domain through the VCO.

$$V_{cont} = A * \cos(2\pi fin * t).\ (\mathrm{A} = 1, \text{for simplicity}). \tag{2}$$

$$V_{outp}(t) = V_0 * \cos\left(w_0 t + kvco \int V_{cont}(t)dt\right). \tag{3}$$

$$V_{outn}(t) = V_0 * \cos\left(w_0 t - kvco \int V_{cont}(t)dt\right). \tag{4}$$

Since what we are interested in is the excess phase, the VCO_p output, $\phi_{excessp}$, can be expressed as equation (5). Similarly, excess phase of VCO_n output, $\phi_{excessn}$, is expressed in equation (6). Then, the total phase difference between the two VCOs are in equation (7).

$$\phi_{excessp} = kvco \int V_{cont}(t)dt. \tag{5}$$

$$\phi_{escessn} = -kvco \int V_{cont}(t)dt. \tag{6}$$

$$\therefore \phi_{excess} = \phi_{excessp} - \phi_{excessn} = 2kvco \int V_{cont}(t)dt. \tag{7}$$

Table. 1 further visualize and simplify the operation of the conventional VCO phase integration. When Time = 1, the output of VCO_p increases by +1 from initial phase 0 (see equation. (5)). Similarly, the output $\phi_{excessn}$ of VCO_n decreases by -1. Therefore, at T =

1, the total phase difference between VCO_p and VCO_n is integrated by 0 to 2 (see equation. (7)). Time = 2, VCO_p is added by +2 with the previous phase condition 0+1. VCO_n is subtracted by -2 from the previous condition 0 - 1. Therefore, at Time = 2, the total phase difference is 6. From the initial phase to T = 2, phase difference experiences 0 → 2 → 6. As it clearly shows that the VCO integrates the inputs and that the VCO itself can act as a loop filter. Additionally, the difference between the current and the previous phase value is proportional to the input. That is, linearly increases in the frequency domain. This is the operating principle of a conventional XOR-DFF based ADC [20].

The proposed direct chopped VCO is explained below. The chopping frequency is expressed in equation (8). The chopping function is multiplied by the input and VCO integrates its voltage input to phase (see equation (10)).

$$f_{ch}(t) = \frac{2}{n\pi * fch}[(-1)^n - 1]\sum_{n=1}^{\infty} \sin(2\pi nt * fch), \qquad f_{ch}(t) * f_{ch}(t) = 1. \tag{8}$$

$$V_{cont} = f_{ch}(t) * \cos(2\pi fin * t). \tag{9}$$

$$V_{outp}(t) = V_0 * \cos\left(w_0 t + kvco \int f_{ch}(t) * V_{cont}(t)dt\right).$$

$$V_{outn}(t) = V_0 * \cos\left(w_0 t - kvco \int f_{ch}(t) * V_{cont}(t)dt\right). \tag{10}$$

After experiencing chopping, phase integration, and demodulation, the final excess phase value, $\phi_{excessp}$ and $\phi_{excessn}$, is derived as equation (11). The phase difference between

the two VCOs is expressed in equation (12).

$$\phi_{excessp} = f_{ch}(t) * kvco \int f_{ch}(t) * V_{cont}(t)dt.$$

$$\phi_{excessn}(t) = -f_{ch}(t) * kvco \int f_{ch}(t) * V_{cont}(t)dt. \quad (11)$$

$$\therefore \phi_{excess}(t) = \phi_{excessp}(t) - \phi_{excessn}(t) = f_{ch}(t) * 2kvco \int f_{ch}(t) * V_{cont}(t)dt. \quad (12)$$

Table2 helps to understand the above equations more clearly. When T = 1 and $f_{ch} = 1$, same scenario with conventional VCO behavior. No chopping, VCO integrates the input phase. Excess phase of VCO_p, $\phi_{excessp}$ = 0 + 1. Similarly, the excess phase of VCO_n, $\phi_{excessn} = 0 - 1$. When T = 2, $f_{ch} = -1$, chopping occurs. V_{inp} goes into VCO_n and V_{inn} goes into VCO_p. $V_{inp} = 2$ goes into VCO_n and $V_{outn} = 0 - 1 + 2$. V_{outn} is demodulated again and the final output becomes $\phi_{excessp} = 0 - 1 + 2$. Likewise, $V_{inn} = -2$ is added to the previous phase value $VCO_p = 0 + 1$ and final value becomes $\phi_{excessn} = 0 + 1 - 2$.

Time	1	2	3	4
Input	1	2	3	4
$f_{ch}(t)$	1	1	1	1
$\phi_{escessp}$	0 + 1	0 + 1 + 2	0 + 1 + 2 + 3	0 + 1 + 2 + 3 + 4
$\phi_{escessn}$	0 - 1	0 - 1 - 2	0 - 1 + 2 - 3	0 - 1 - 2 - 3 - 4
ϕ_{escess}	0 → 2	2 → 6	6 → 12	12 → 20
$\phi(t) - \phi(t-1)$	2	4	6	8

Table. 1. Conventional VCO

Time	1	2	3	4
$f_{ch}(t)$	1	-1	1	-1
$\phi_{escessp}$	0 + 1	0 – 1 + 2	0 + 1 - 2 + 3	0 - 1 + 2 - 3 + 4
$\phi_{escessn}$	0 - 1	0 + 1 - 2	0 - 1 + 2 - 3	0 + 1 - 2 + 3 - 4
ϕ_{escess}	0 → 2	-2 → 2	-2 → 4	-4 → 4
$\phi(t) - \phi(t-1)$	2	4	6	8

Table. 2. Proposed direct chopped VCO

One drawback is that the VCO phase difference (see ϕ_{excess} from Table. 2) no longer integrates input continuously. Consequently, the proposed chopped VCO technique can be only used in frequency domain ADC. When T = 1, ϕ_{excess} increases from 0 to 2. However, chopping occurs at T = 2, and ϕ_{excess} increases -2 to 2. Phase difference flows 0 → 2(0+2), chopping, -2(0-2) → 2(0-2+4). This scenario is different from the conventional structure. In conventional case, phase difference flows 0 → 2(0+2) and 2→ 6(0+2+4). Therefore, the chopped VCO cannot act as a continuous loop filter. However, since $\phi(t) - \phi(t-1)$ is linear to input. That is, the direct chopped VCO structure can be used as an ADC when information is quantized in the frequency domain. A more detailed explanation is provided in Appendix 1.

2.2.2 Error Caused by Chopping

By directly applying chopping to the VCO, the 1/f noise of the VCO is eliminated. However, it has a trade-off. The 1st order noise-shaping does not occur at every chopping clock. And that periodic error makes flat noise, although most of the quantization noise is 1st order shaped at every sampling frequency. Figure. 2.3. shows a conceptual explanation of the periodic error. T = 1, figure.2 is a conventional 1st order noise shaping situation. Quantization error can be derived as [21], where N is the number of the VCO phase, $\Phi_x(n)$ is the VCO phase change due to the analog input and $\Phi_q(n)$ is the quantization error.

$$Y(z) = \frac{N}{2\pi}\left(\Phi_x(z) + (z^{-1} - 1)\Phi_q(z)\right). \quad (13)$$

At T = 3, chopping occurs. The previous phase value is no longer maintained its previous information.

$$Y(z) = \frac{N}{2\pi}\left(\Phi_x(z) + (z^{-1} - 1)\Phi_q(z)\right) + \Phi_{chop,error}(z). \quad (14)$$

That is, flat noise $\Phi_{error}(z)$ occurs and limits noise performance.

Flat noise error caused by the chopping technique, $\Phi_{chop,error}$, can be derived using a conventional quantization scenario. Equation (15) is a well-known equation of quantization error [21].

$$\Delta = \frac{2\pi}{M * k_{vco} * t_s}. \; E_n(t) = \frac{\Delta}{t_s}t.$$

$$P = \frac{1}{t_s}\int_{-\frac{Ts}{2}}^{\frac{Ts}{2}} E_n^2(t)dt = \frac{\Delta^2}{12}.$$

$$\therefore Q_e = \frac{\Delta^2}{12f_s}. \quad (15)$$

Delta (Δ) is the LSB of quantization error. P is the total value of the quantization error overall frequency. In-band quantization error is obtained by dividing P by the sampling frequency f_s (= 1/t_s). Based on this, $\Phi_{chop,error}$ can be derived. In the proposed technique, the delta is the same as the conventional one. The only difference is the periodic time. In the proposed technique, quantization error occurs every f_{ch}, not f_s. Therefore, $Q_{fch,error}$ is expressed in equation. (16). Simply dividing equation (15) with m. Note that error occurs rising and falling edge of chopping frequency so that 2 should be multiplied. By lowering

f_{ch} and increasing k_{vco}, $Q_{fch,error}$ can be designed lower than targeting noise.

$$t_{ch} = m \cdot t_s.$$

$$P_{fch,error} = \frac{2}{mt_s}\int_{-\frac{t_s}{2}}^{\frac{t_s}{2}} E_n^2(t)dt = \frac{\Delta^2}{6 \cdot m}.$$

$$\therefore Q_{fch,error} = \frac{\Delta^2}{6 \cdot mf_s} = \frac{2 \cdot \pi^2 \cdot f_{ch}}{3 \cdot M^2 \cdot {k_{vco}}^2}. \quad (16)$$

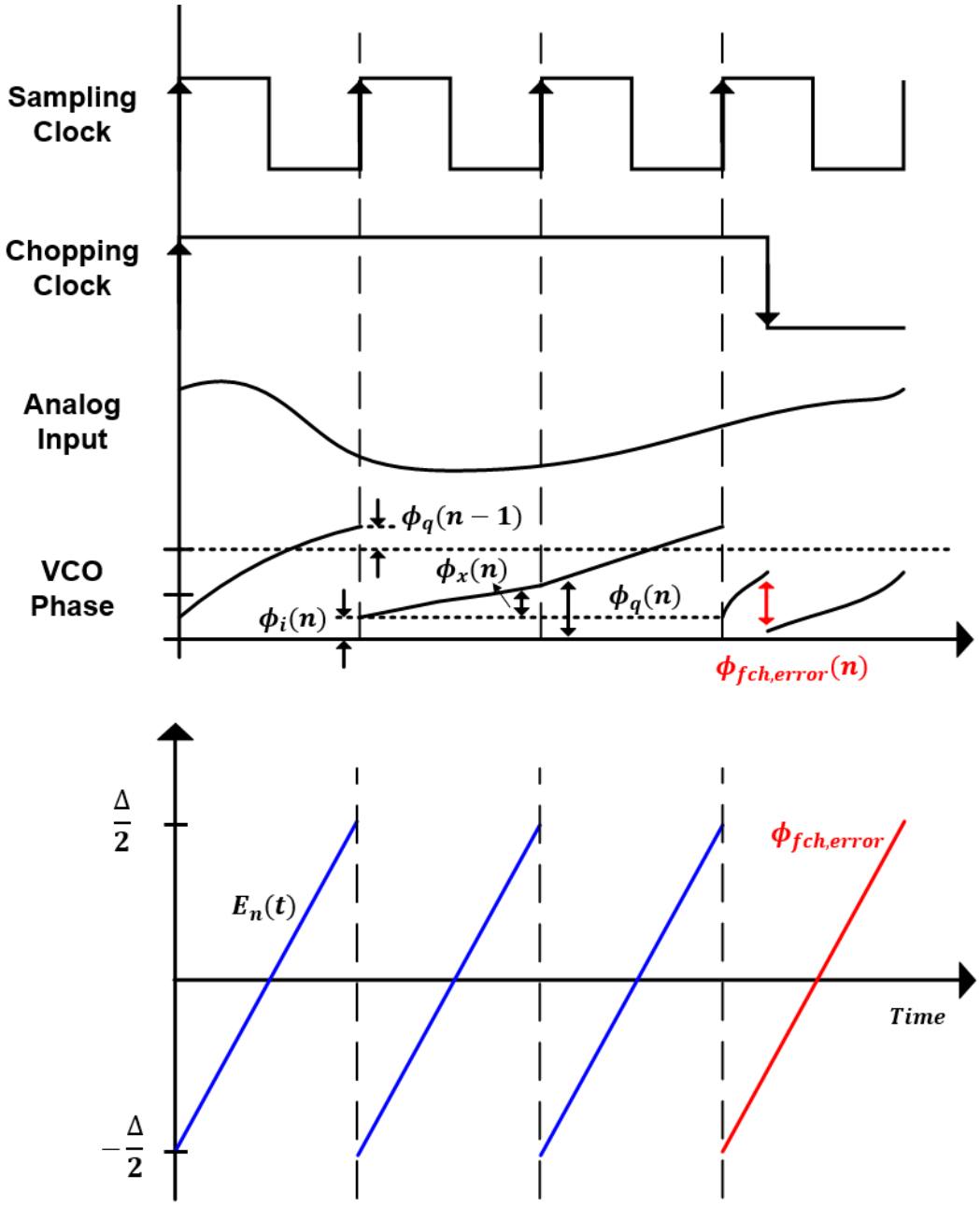

Figure. 2.3. Conceptual explanation of 1st order noise shaping and error caused by chopping (top), operation timing diagram of quantization error caused by chopping (bottom)

2.3 VCO Quantizer

A counter-based quantizer is adopted to quantize information. The commonly used XOR-DFF based quantizer cannot meet SNR performance due to insufficient signal gain. A counter-based quantizer measures the difference between the two VCOs' cycles during two consecutive sampling frequencies. Therefore, the sampling frequency can be significantly lower than the VCO center frequency, and the signal has a large gain thanks to lowered fs. The counter counts the number of positive edges of VCO during one sampling clock and stores it in DFF. The counted value indicates how many phases of VCO have changed.

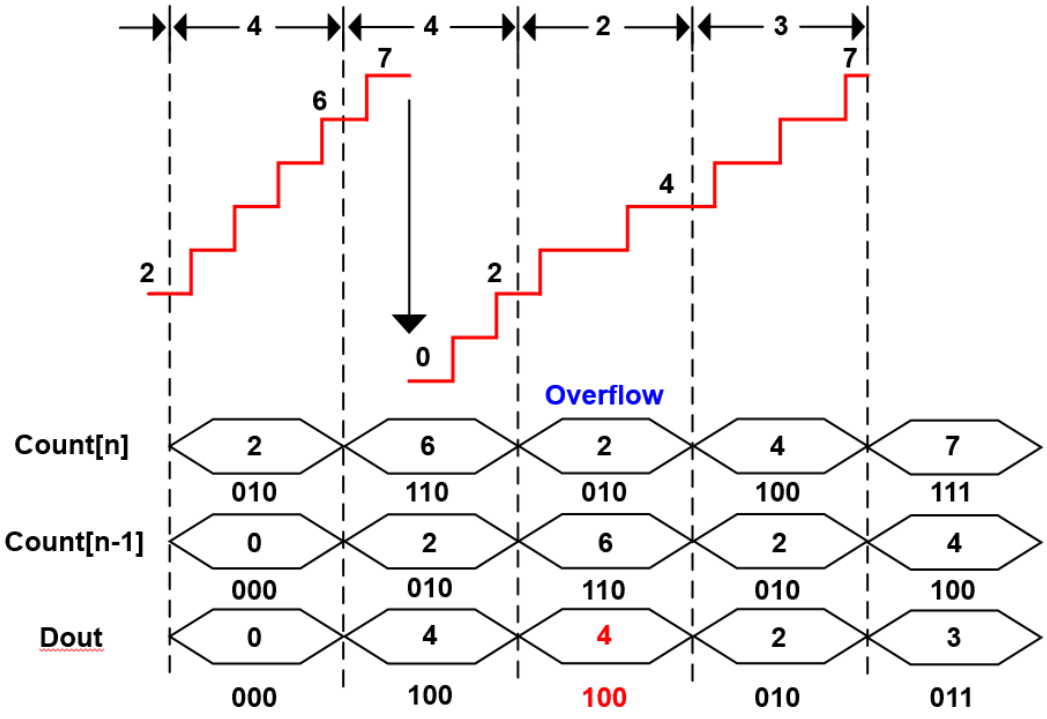

Figure. 2.4. Example of roll-over counter

A differentiator is used to subtract stored values to determine the frequency information in the digital domain. Notice that the reset counter is not used, which reset information at every fixed frequency. Instead, a roll-over counter is employed to eliminate the detrimental

effects of finite reset time on noise shaping [22]. As a result, counter output overflows but does not pose a problem.[23] Fig. 2.4. illustrates how subtraction can retrieve the right frequency output. Dout = 4, which is the correct digital output even though there was an overflow. Note that output is delayed by one clock due to DFF.

2.4 Bootstrapped Chopper

MOS switches suffer from a number of imperfections. Such devices exhibit an input-dependent on-resistance, thereby introducing distortion. Additionally, low supply voltage worsens distortion. This issue can be resolved by bootstrapped chopper. A circuit technique that minimizes the switch on-resistance variation in the presence of large input and output voltage swings. Using this technique, the switch's gate voltage can rise above the supply voltage so that minimize distortions.

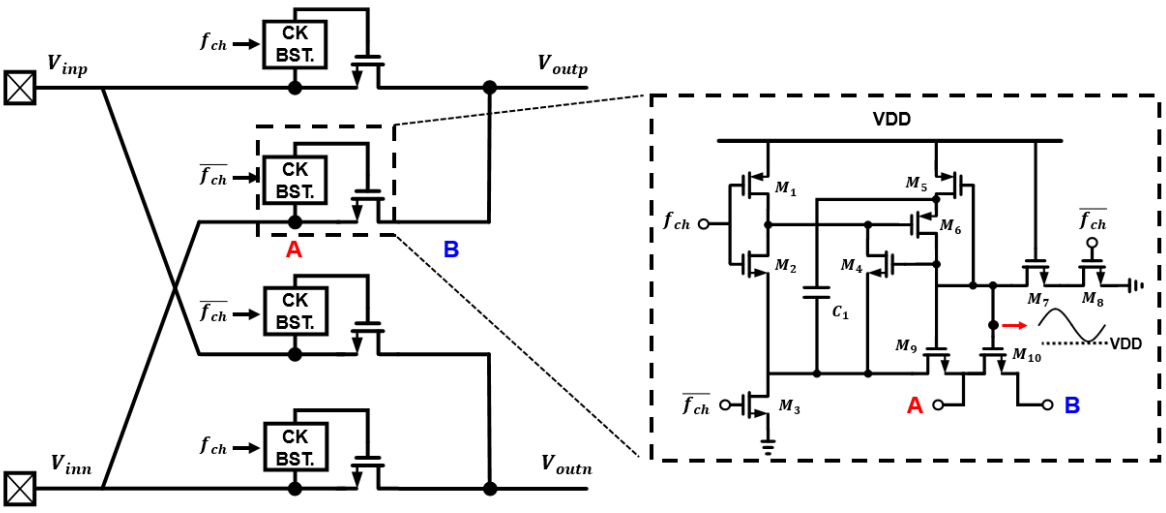

Figure. 2.5. Schematic of bootstrapped chopper

Figure. 2.5. illustrates the bootstrapped chopper. The basic operation is that C1 is precharged to VDD. Then, the input signal is sampled. M10 gate voltage maintain its voltage

VDD. Consequently, M10 on-resistance becomes stable. When sampling is done, M8 turns on thus M10 switches turns off.

2.5 Bulk-driven VCO Design

VCO's phase noise and non-linearity determine the overall ADC performance. Therefore, the VCO is designed to have low noise and high linearity. Bulk-driven VCO was used to meet overall performance [24]. The VCO consists of an odd number (N) of inverters. Assuming NMOS and PMOS drive equal current, the signal will be delayed by the time t_d in each inverter, and the output frequency of the oscillator is given from:

$$f = \frac{1}{2Nt_d}$$

Each node of VCO has a capacitance C_L, consisting of the total gate, drain capacitance from two transistors, routing capacitance, and parasitic capacitance. If the number of VCO stage is large enough, C_L will be completely charged and discharged during one period. The total charge will be $Q = C_L V_{dd}$. Assuming the transistor charges the capacitance with an approximately maximum current I_d, then the frequency of the VCO is given by

$$f = \frac{I_d}{2NC_L V_{dd}}$$

I_d can be controlled in different ways. Current starved Ring VCO(RVCO) techniques are

often used [25]. This approach results in a wide tuning range. However, this approach suffers from a highly non-linear property. Another way to control I_d is to change the threshold voltage of the transistors through bulk voltage. This principle yields better linearity [24]. Furthermore, this technique implies a high input impedance because input sees only parasitic capacitance related to the transistor's body. It is also possible to have a rail to rail inputs. The bulk-driven technique has been shown to have a very low supply voltage and low power consumption capabilities [27].

The following equation compares k_{vco} two VCOs structure, current starved RVCO, and bulk-driven VCO. Note that high linearity means a constant k_{vco}.

$$\frac{df}{dV_{gs}} = k_{VCO} = \frac{1}{CV_{dd}} \cdot \frac{dI_d}{dV_{gs}} = \frac{g_m}{CV_{dd}}$$

$$\frac{df}{dV_{ctrl}} = k_{VCO} = \frac{1}{CV_{dd}} \cdot \frac{dI_d}{dV_{bs}} = \frac{g_{mb}}{CV_{dd}}$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_F - V_{bs}}}, \qquad (17)$$

Where γ is a process value and ϕ_F is the surface potential of the MOS transistor. Equation (17) shows that g_{mb} is g_m power higher lower than one. Thus, bulk-driven experience fewer changes so that bulk-driven VCO has better linearity.

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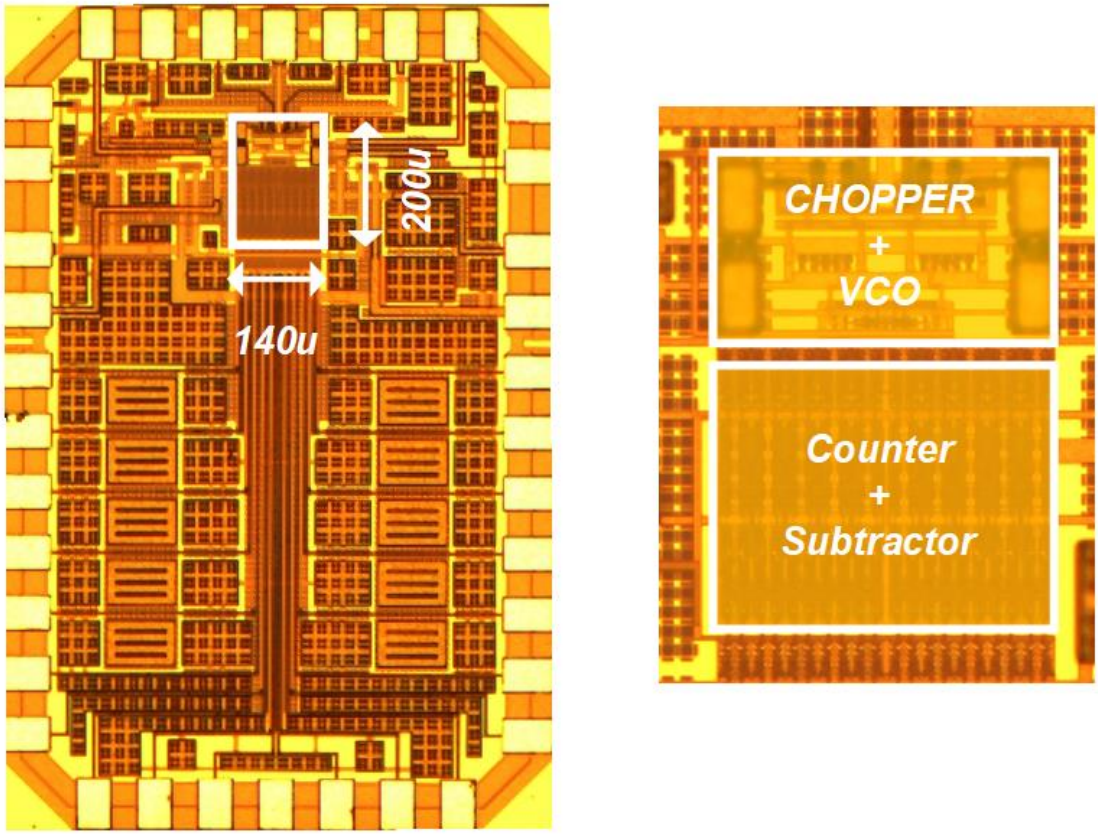
III. Measurement Results

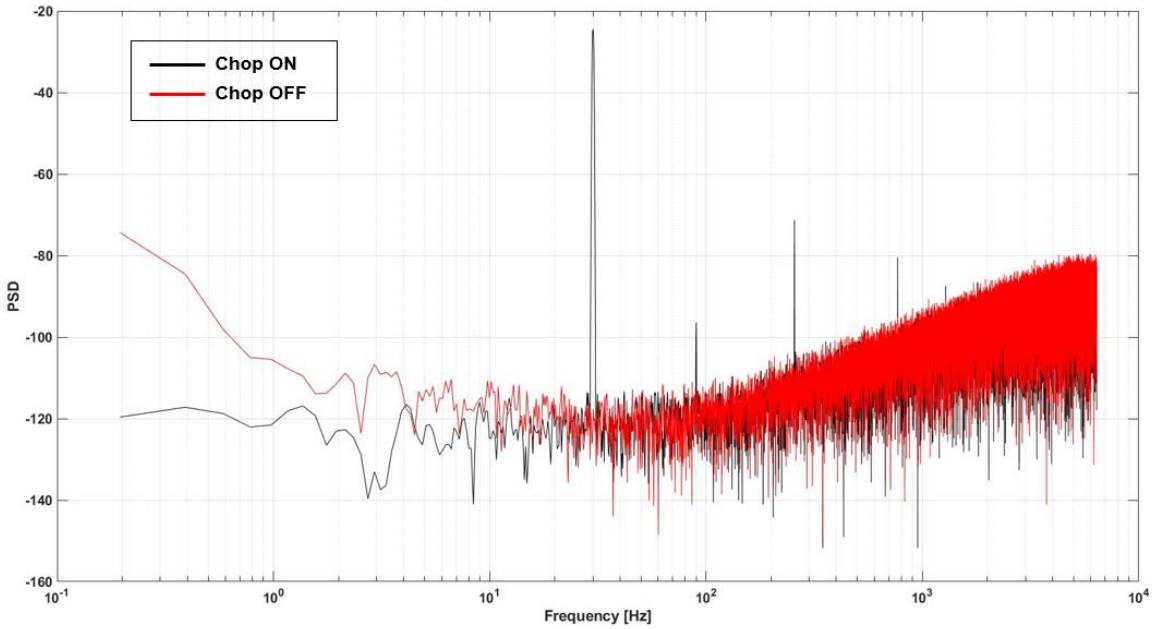
A prototype of the proposed VCO-based ADC is fabricated in 180-nm CMOS technology. The die photograph is in Fig. 3.1. The proposed ADC only occupies an area of 0.028mm^2



thanks to the digital intensive structure.

Figure. 3.1. Die photograph

Fig. 3.2. shows the measured output spectrum with a 30Hz 60mVpp input signal. The proposed direct VCO chopping technique is ON and OFF. When chopping is disabled, the 1/f noise of VCO is a dominant noise source and limit SNDR. Enabling the chopping technique, 1/f noise is reduced. Thanks to the bulk-driven VCO an SFDR of 72 dB is achieved with no additional blocks. Note that tones in 256Hz is that offset caused by mismatch and



modulated to out of bandwidth.

Figure. 3.2. Measured output PSD

The SNDR is measured and the results are shown in Fig. 3.3. SNDR performance is 66.56dB at 70mVpp input. Note that VCO allows input amplitude up to supply voltage so that the proposed ADC can tolerate large DC electrode offset.

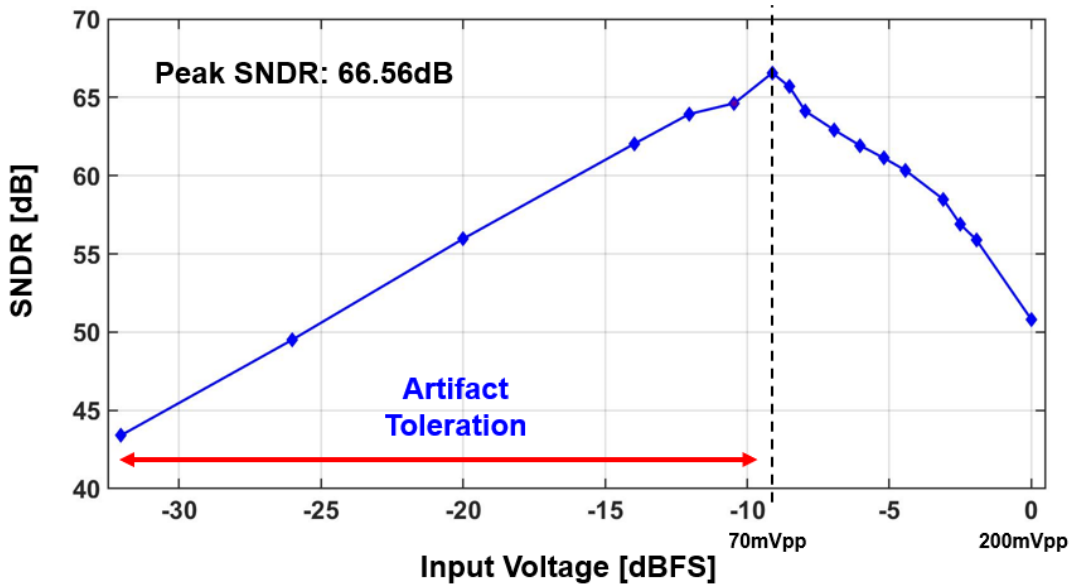
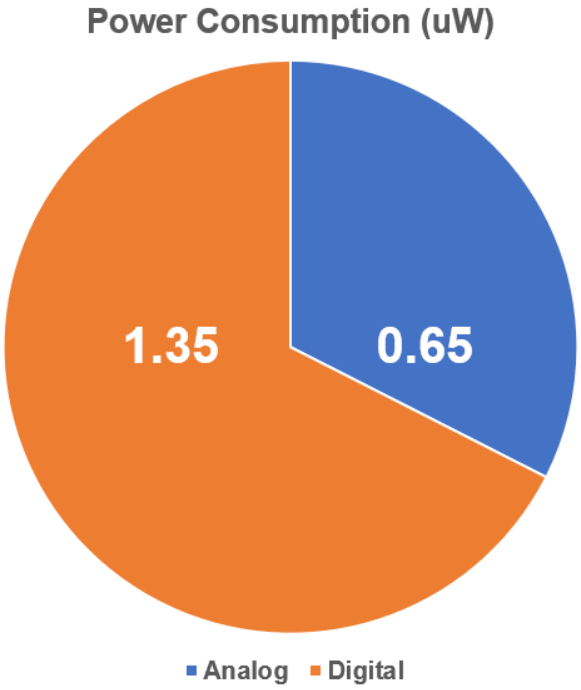


Figure. 3.3. Measured SNDR performance

Operating under 0.5V analog (chopper, VCO) and 0.6V digital (counter, subtractor) supplies and at the nominal 70mVpp input, the ADC prototype consumes 2μW when sampling frequency at 12.8kHz. Fig. 3.4. shows the power breakdown when operating at the 70mVpp input, the analog and digital blocks (counter, subtractor) consume 0.65 and



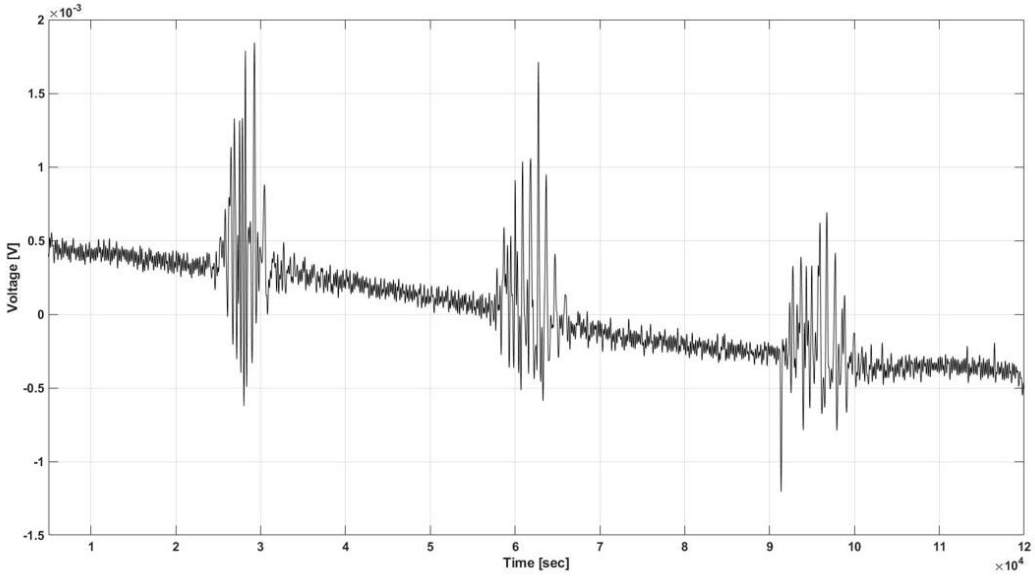
1.35uW respectively.

Figure. 3.4. Power breakdown diagram

The IRN PSD is 22uVrms with BW 200Hz. The overall noise performance is dominated by the chopping error. The measured in-band CMRR is 68dB. The high CMRR suggests that the proposed ADC can direct digitizing input signals without needing an OTA.

To demonstrate the proposed VCO based ADC, a three-lead on-body EMG recording is performed. Fig. 3.5. shows the waveform. The signal leads are directly connected to the sensor readout differential input, while the reference electrode is connected to the half supply voltage. The 60Hz signal is notched out using MATLAB digital filter. The chopping

frequency applied for EMG, EMG measurement is 256Hz and the input impedance is



larger than 1Gohm.

Figure. 3.5. Measured EMG waveform

Table. 3. provides a comparison table. This paper achieves a peak Schreier FoM of 144.6dB. The scaling-friendly architecture, its area is only 0.028mm^2 in 180nm technology. The input impedance of this paper also shows good performance without any additional input impedance boosting technique.

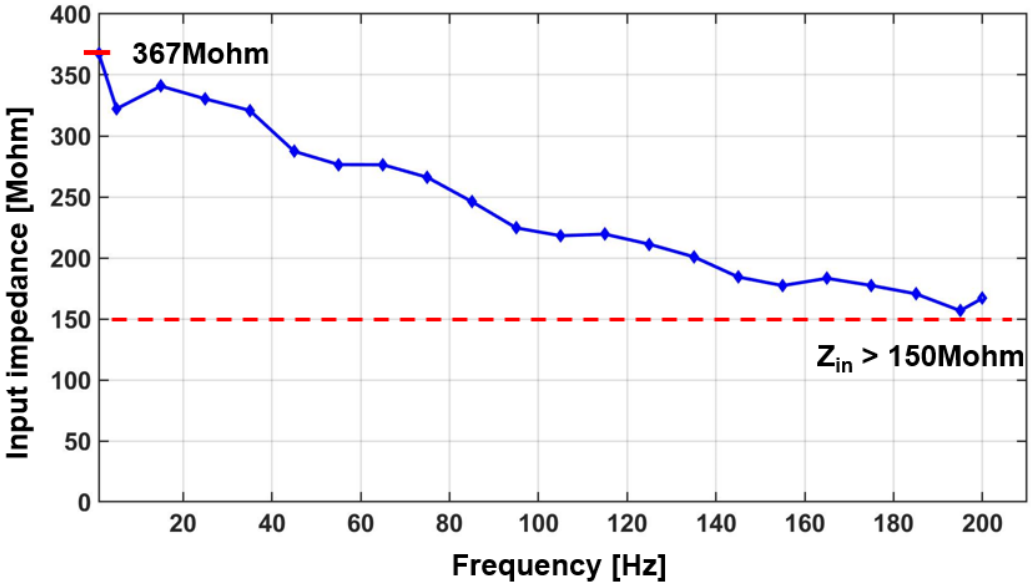


Figure. 3.6. Simulation result of the input impedance

Reference	[1] ISSCC'16	[2] JSSC'17	[3] JSSC'17	[4] CICC'18	This work
Topology	VCO-ADC(Open)	VCO-ADC(Open)	TDC based AFE	IA-SAR	VCO-ADC(open)
Technology	40nm	40nm	40nm	40nm	180nm
Need OTA	No	Yes	Yes	Yes	No
Noise Shaping	X	1st	X	X	1st
Chopping	X	O	O	O	O
Supply	1.2V (A) 0.45V (D)	1.2V	0.6V	0.6V	0.5V (A) 0.6V (D)
Power/ch	7μW	17μW	3.3μW (only AFE)	3.8μW (ECG+BioZ)	2μW
Fs	3kHz	4.2MHz	25MHz	20kHz	12.8kHz
Bandwidth	200Hz	5kHz	150Hz	150Hz	200Hz
In-ref. Noise (BW 200)	5.2uVrms	0.45uVrms	23uVrms	2.14uVrms	22uVrms
Input Range	±50mV	±8mV	±40mV	±200mV	±35mV
SFDR	79dB (after NLC)	**61dB	56dB	**62dB	72dB
SNDR	74dB	61.85dB	55.9**	60.2	66.56dB
Z_{in}(@10)	∞(@DC)	70MΩ	50MΩ	140MΩ	340MΩ
*FoM_S	148.6	146.5	132.5**	136	146.56
Area	0.135mm²	0.0145mm²	0.015mm² (+Offchip filter)	**0.25mm²	$0.028mm^2$

* FoM_S = SNDR +10*log10(BW/Power) **estimated

Table. 3. Comparison Table

IV. Conclusion

This paper presented an VCO-based ADC for EMG acquisition. The VCO-based ADC achieves 1st order noise shaping and sufficient gain to enhance SNR. To eliminate the 1/f noise of VCO, the direct chopped VCO technique is implemented. However, it occurs error at every chopping frequency as a trade-off. VCO can tolerate large artifact from 0 to 200mVpp. This article achieves area efficient, low power, large input impedance for multi-channel, non-invasive EMG monitoring.

Appendix I.

At T = 1, the output value $\phi_{escess}(1)$ is a phase difference between VCO_p and VCO_n. When T = 2, chopping occurs and $-\phi_{escess}(1)$ becomes the initial phase difference. At the end of T = 2, the final phase difference is $\phi_{escess}(2)$. We can say that phase difference changes from $-\phi_{escess}(1)$ to $\phi_{escess}(2)$. At T = 3, chopping occurs again and the initial phase difference value will be $-\phi_{escess}(2)$. Similarly, at the end of T = 3, phase difference changes from -$\phi_{escess}(2)$ to $\phi_{escess}(3)$. The overall phase difference can be represented as $\phi_{escess}(t+1) - (-\phi_{escess}(t))$. Equations are derived below.

$$\phi_{escess}(t) = \phi_{escessp}(t) - \phi_{escessn}(t) = f_{ch}(t) * 2kvco \int f_{ch}(t) * V_{cont}(t)dt.$$

$$V_{out}(t+1) = \phi_{escess}(t+1) - \left(-\phi_{escess}(t)\right) = \phi_{escess}(t+1) + \phi_{escess}(t)$$

$$= f_{ch}(t+1) * 2kvco * Ts * \sum_{0}^{t+1} f_{ch}(t) * V_{cont}(t) + f_{ch}(1) * 2kvco * Ts * \sum_{0}^{t} f_{ch}(t) * V_{cont}(t)$$

$$if, \quad f_{ch}(2n+1) = 1, \quad f_{ch}(2n) = -1, \quad n \geq 0, \quad (n = integer)$$

$$V_{out}(t+1) = \phi_{escess}(t+1) + \phi_{escess}(t)$$

$$= f_{ch}(t+1) * 2kvco * Ts * \sum_{0}^{t+1} f_{ch}(t) * V_{cont}(t) + f_{ch}(1) * 2kvco * Ts * \sum_{0}^{t} f_{ch}(t) * V_{cont}(t)$$

$$= (+1) * 2kvco * Ts * [-V_{cont}(0) + V_{cont}(1) - V_{cont}(2) \dots - V_{cont}(t) + V_{cont}(t+1)]$$

$$+(-1) * 2kvco * Ts * [-V_{cont}(0) + V_{cont}(1) - V_{cont}(2) \dots + V_{cont}((t-1)) - V_{cont}(t)]$$

$$= 2kvco * Ts * V_{cont}(t+1)$$

$$if, \quad f_{ch}(2n+1) = -1, \quad f_{ch}(2n) = 1, \quad n \geq 0, \quad (n = integer)$$

$$V_{out}(t+1) = \phi_{escess}(t+1) + \phi_{escess}(t)$$

$$= f_{ch}(t+1) * 2kvco * Ts * \sum_{0}^{t+1} f_{ch}(t) * V_{cont}(t) + f_{ch}(1) * 2kvco * Ts * \sum_{0}^{t} f_{ch}(t) * V_{cont}(t)$$

$$= (-1) * 2kvco * Ts * [V_{cont}(0) - V_{cont}(1) + V_{cont}(2) \dots + V_{cont}(t) - V_{cont}(t+1)]$$

$$+(+1) * 2kvco * Ts * [+V_{cont}(0) - V_{cont}(1) + V_{cont}(2) \dots - V_{cont}(t-1) + V_{cont}(t)]$$

$$= 2kvco * Ts * V_{cont}(t+1)$$

$$\therefore \frac{V_{out}}{V_{cont}}(t) = 2kvco * Ts$$

Therefore, the direct chopped VCO technique can be used when information is quantized in the frequency domain.

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요 약 문

다채널, 비침습형 근전도 측정을 위한 높은 입력 임피던스를 갖는 전압제어발전기 기반 노이즈 쉐이핑 아날로그 디지털 컨버터

다채널, 비침습형 근전도 측정을 위해 전력, 면적, 입력 임피던스는 중요한 파라미터이다. 또한 1/f 노이즈와 비선형성에 의한 3 차 고조파도 고려해야 한다. 최근, 위의 문제를 다루면서도, 디지털 집적으로 회로의 효율을 높인, VCO 기반의 ADC 가 주목되어져 왔다. 하지만 여전히, 1/f 노이즈, 입력 임피던스, 면적 문제를 가지고 있다.

이 연구는 가장 간단한 방식으로 위의 문제를 해결하는데 초점을 두고 있다. VCO 에 chopping 을 직접 적용해서 1/f noise 를 제거한다. 하지만 단점으로써 일정주기마다 잡음을 발생하고, 이는 전체 구조의 잡음 성능을 저하시킨다. DC-coupled 입력은 입력에서 보이는 기생 캐패시턴스가 VCO 의 bulk 로만 구성하게 만든다. 따라서 입력 임피던스를 1Gohm 까지 얻는다. 개회로 기반의 ADC 구조와 아날로그 블락의 제거는 폐회로에서 고려해야 하는 안정성, 복잡성, 전력 문제를 없애고, 면적을 0.028mm^2 로 줄인다. 또한 입력 시그널을 VCO 의 bulk 에 연결함으로써 추가적인 테크닉 없이도 72dB 의 SFDR 성능을 얻었다.

핵심어: 다채널, 비침습, EMG, 입력 임피던스, VCO 기반 ADC