

ADVANCED MATERIALS

Probing Optical Multi-Level Memory Effects in Single Core-Shell Quantum Dots and Application Through 2D–0D Hybrid Inverters

Hyun-Soo Ra, Tae Wook Kim, Derrick Allan Taylor, Je-Jun Lee, Seungho Song, Jongtae Ahn, Jisu Jang, Takashi Taniguchi, Kenji Watanabe, Jae Won Shim, Jong-Soo Lee,* and Do Kyung Hwang*

Challenges in the development of a multi-level memory (MM) device for multinary arithmetic computers have posed an obstacle to low-power, ultra-high-speed operation. For the effective transfer of a huge amount of data between arithmetic and storage devices, optical communication technology represents a compelling solution. Here, by replicating a floating gate architecture with CdSe/ZnS type-I core/shell quantum dots (QDs), a 2D-0D hybrid optical multi-level memory (OMM) device operated is demonstrated by laser pulses. In the device, laser pulses create linear optically trapped currents with MM characteristics, while conversely, voltage pulses reset all the trapped currents at once. Assuming electron transfer via the energy band alignment between MoS₂ and CdSe, the study also establishes the mechanism of the OMM effect. Analysis of the designed device led to a new hypothesis that charge transfer is difficult for laterally adjacent QDs facing a double ZnS shell, which is tested by separately stimulating different positions on the 2D-0D hybrid structure with finely focused laser pulses. Results indicate that each laser pulse induced independent MM characteristics in the 2D-0D hybrid architecture. Based on this phenomenon, we propose a MM inverter to produce MM effects, such as programming and erasing, solely through the use of laser pulses. Finally, the feasibility of a fully optically-controlled intelligent system based on the proposed OMM inverters is evaluated through a CIFAR-10 pattern recognition task using a convolutional neural network.

1. Introduction

The emergence of the Internet of Things and smart robots has created a flood of data, and in order to keep up with all the related trends, the development of nextgeneration data storage devices has garnered extensive research interest. In addition to advances in the integration of many transistors in a narrow area by implementing ever narrower line widths to increase data storage capacity, industry is currently aimed at multi-stacked NAND memory devices while research fields are focused on designing multi-level memory (MM) devices for the creation of a multinary computer (MC).^[1] One promising building block for MCs is 2D semiconductor heterojunctions such as graphene, transition metal dichalcogenides (TMDs), and black phosphorus, which offer a number of advantages. First, a staggered-type 2D heterojunction induces a negative differential resistance that plays a role in ternary and quaternary inverters.^[1f,i,2] Second, defect engineering between semiconductor channels

H.-S. Ra, T. W. Kim, S. Song, J. Ahn, J. Jang, D. K. Hwang
Center for Opto-Electronic Materials and Devices, Post-Silicon
Semiconductor Institute, Korea Institute of Science and Technology (KIST)
Seoul 02792, Republic of Korea
E-mail: dkhwang@kist.re.kr
T. W. Kim, J. W. Shim
School of Electrical Engineering
Korea University
Seoul 02841, Republic of Korea
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adma.202303664
© 2023 The Authors. Advanced Materials published by Wiley-VCH
CmbH. This is an open access article under the terms of the Greative

GmbH. This is an open access article under the terms of the Creative Commons Attribution-NonCommercial License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited and is not used for commercial purposes.

DOI: 10.1002/adma.202303664

D. A. Taylor, J.-S. Lee Department of Energy Science and Engineering, Daegu Gyeongbuk Institute of Science and Technology (DGIST) Daegu 42988, Republic of Korea E-mail: jslee@dgist.ac.kr J.-J. Lee Center for Spintronics, Korea Institute of Science and Technology (KIST) Seoul 02792, Republic of Korea T. Taniguchi, K. Watanabe Advanced Materials Laboratory, National Institute for Materials Science Tsukuba 305-0044, Japan D. K. Hwang Division of Nanoscience & Technology, KIST School, University of Science and Technology (UST) Seoul 02792, Republic of Korea D. K. Hwang KU-KIST Graduate School of Converging Science and Technology Korea University Seoul 02841, Republic of Korea

CIENCE NEWS



Figure 1. 2D–0D hybrid memory device structure and HR-TEM with EDS mapping results. a) Conventional floating gate architecture based on a dielectric layer, MoS₂, and metal. b) Mimic diagram of the floating gate (red) / dielectric layer (blue) made up of CdSe/ZnS core/shell QDs. Ligand exchange of QDs is required for improving charge transfer. c) Schematic diagram of the designed 2D–0D hybrid OMM device and operation strategy. The yellow and black spheres are sulfide and molybdenum, respectively, and the green layer is the h-BN dielectric layer. d) HR-TEM image of CdSe/ZnS core/shell QDs and EDS mapping image of S, Zn, Se, and Cd shown in different colors. Scale bar is 10 nm. e) Line scan profile of a single QD reflecting the elemental composition of the core. f) HR-TEM image of CdSe/ZnS QDs and MoS₂. g) HR-TEM and h) EDS mapping images of the 2D–0D hybrid interface for observing the ZnS shell thickness (3 to 3.5 nm) and the real distance (under 1 nm) between MoS₂ and the CdSe core, where Mo is shown in yellow, Zn in blue, and Cd in red. Scale bar is 5 nm.

and dielectric layers induces a charge trapping effect via electric field pulses, demonstrating the potential for MM.^[3] Third, in lateral and vertical TMD channels, mobile ions from the electrode metal form atomic-scale filaments inside the 2D materials, the thickness of which can be tuned as a function of applied voltage pulse.^[1h,4] The metal filament thickness determines the variable resistance step, which is reversible. However, the cuttingedge technology as above has difficulties in doping level control and large-scale fabrication with integrated complementary circuits. Even though MC technology can improve energy dissipation and arithmetic computing speed, it has a speed limit in transmitting a huge amount of data through electrical signal processing. To overcome this limitation, optical communication between the arithmetic unit and the storage unit of the MC is thought to provide the best solution.^[5] Mixed-dimensional hybrid structures have accordingly been attracting attention as a key constituent to realize optical memory effects.^[6] For instance, 3D oxide semiconductors have a flexible charge trap site, 2D materials have excellent carrier mobility, and 0D materials have an excellent light absorption coefficient and long exciton lifetime. Among various forms of mixed-dimensional hybrids, 2D-0D hybrid structures in particular have demonstrated optical memory effects, but to date, these structures have been operated by optical/electrical pulses such as laser pulse programming with electrical pulse erasing.^[7] To be specific, laser pulse erasing has yet to be reported.

In the present work, we observe for the first time a 2D–0D hybrid-based optical multi-level memory (OMM) effect. The hybrid structure consists of MoS_2 as the channel material and CdSe/ZnS core/shell quantum dots (QDs) with a ZnS shell of

10 layers of acting as a floating gate unit, where a sufficiently thick ZnS shell is thought to act as a stable charge trap inside the CdSe core. We hypothesize that a single QD has the ability to maintain different memory levels because there is no charge leakage between the QDs in the designed structure. In order to prove this, we stimulated different positions on a 2D-0D hybrid OMM device with a focused laser pulse (<1 μ m) and found that the different positions exhibited independent OMM effects in a linear manner. Based on this novel finding, we propose an OMM inverter consisting of two 2D-0D hybrid OMM devices to implement highly linear programming and erasing processes only using laser pulses of the same wavelength. Finally, using a convolutional neural network composed of the OMM inverter set, we evaluated the feasibility of applying the inverters as synapses in a fully optically-controlled intelligent system via training and inference tasks using the CIFAR-10 dataset (Canadian Institute for Advanced Research).

2. Results and Discussion

2.1. 2D-0D Hybrid OMM Device Structure

The design of the 2D–0D hybrid OMM device originated from a floating gate unit. As depicted in **Figure 1**a, the conventional floating gate structure has a dielectric layer consisting of a tunneling barrier and a control barrier with a floating gate metal between them that traps electrons and holes from the channel.^[8] This floating gate unit is considered here to be analogous to type-I core/shell QDs. But since charge transfer and trapping at the

IDVANCED MATERIALS

2.2. Optical Multi-Level Memory Characteristics

2D-0D hybrid interface should be achieved with laser pulses only, an optimized shell thickness is required. The particular QDs to replace the floating gate unit were selected as air-stable CdSe/ZnS QDs.^[9] In our previous work, a MoS₂/CdSe-core hybrid structure showed a high responsivity based on the photogain effect and a fast photoresponse but without trapping effects.^[10] For a strong charge coupling effect between MoS₂ and CdSe/ZnS QDs, oleic acid (OA) ligands with long carbon lengths on the surface of the QDs were replaced with short tetrabutylammonium iodide (TBAI) ligands, as shown in Figure 1b. To test different shell thicknesses, we synthesized CdSe QDs with ZnS shells of 0, 2, 5, and 10 layers and investigated the photoluminescence spectra. As the number of ZnS layers increased, we observed an increase in the full width at half maximum (FWHM) from 25 to 50 nm, indicating an increase in particle size variation (see Figure S1, Supporting Information). Scanning transmission electron microscopy (STEM) measurements further supported this observation, showing an increase in particle size from 3.28 \pm 0.23 nm for CdSe to 9.51 \pm 0.82 nm for CdSe/ZnS with ten layers (see Figure S2-1, Supporting Information). However, for the use of QDs as a 0D floating gate structure, ZnS layers that are too shallow exhibit a high tunneling probability, leading to excessive leakage from the QDs (see Figure S6-1,S6-2, Supporting Information). Therefore, we selected ten layers of ZnS as the optimized condition for OMM device fabrication. A memory matrix was then fabricated by integrating CdSe/ZnS QDs onto a MoS₂ field-effect transistor (FET) via layer-by-layer ligand exchange.^[11] Figure 1c shows a schematic diagram of the complete 2D-0D hybrid OMM device. In contrast to conventional floating gate structured devices that rely on the application of an electric field to exhibit MM, the key distinction of our 2D-0D hybrid OMM device lies in its capacity to effectively demonstrate MM using finely tuned optical pulses. This notable distinction highlights the exceptional capability of our device, which will be further elucidated in the subsequent sections of the paper. Figure 1d presents high-resolution transmission electron microscopy (HR-TEM) and energy-dispersive X-ray spectroscopy (EDS) images for a surface analysis of the composite CdSe/ZnS QDs. In the HR-TEM image, the high-contrast center area of each QD is the CdSe core, which is surrounded by the ZnS shell with relatively lower contrast. Figure 1e shows a line scan profile reflecting the elemental composition obtained from a single QD. Since the positions of the Cd/Se and Zn/S atoms are opposite, the quantum well characteristic of type-I QDs is identified in the atomic line profile of the single QD cross-section. The cross-section of the hybrid structure was also analyzed via focused ion beam (FIB)-treated HR-TEM to observe the interface and crystalline structures between MoS₂ and CdSe/ZnS. The HR-TEM image in Figure 1f and Figure S2-1, S2-2 (Supporting Information) illustrates the high crystalline quality of the CdSe/ZnS QDs and MoS₂ layer. Furthermore, the gap between MoS₂ and CdSe/ZnS is under 1 nm is shown in Figure 1g, which supports ligand exchange from long- to short-chain. Finally, as shown in the EDS image in Figure 1h, the hybrid interface between MoS₂ (yellow) and CdSe (red)/ZnS (blue) imitates the floating gate unit depicted in Figure 1a. The thickness of the ZnS shell with ten layers is only \approx 3 to 3.5 nm; considering that photoinduced charges must be transported without electrical control, this thickness should be less than the conventional tunneling barrier thickness, 4 to 6 nm.

In the designed device, the multilayer MoS₂ as a partner material easily accepts electrons from the CdSe cores. In addition, its wide bandgap of 1.3 eV enables the gate electric field of the FET to effectively control the Fermi level, which allows the optimum condition for electron transfer from CdSe to MoS₂.^[12] In order to minimize the dielectric/semiconductor interface trap effect caused by the gate electric field, h-BN as the 2D dielectric material was used as the gate dielectric layer.^[13] Figure 2a shows images of an as-fabricated multilayer MoS₂ FET with h-BN and a 2D-0D FET integrated with CdSe/ZnS QDs. The thicknesses of the MoS₂, h-BN, and QD layers are estimated to be 81, 91, and 52 nm, respectively, from HR-TEM measurement of the crosssection of the channel region (see Figure S2-3, Supporting Information). We have formed the QD layer with sufficient thickness to ensure uniformity. The ZnS shells have a bandgap \approx 3.5 eV. In terms of the MoS₂, ZnS is a quasi-dielectric material through that a negligible leakage current ($\approx 10^{-12}$ A) flows among all electrodes, as shown with the dashed line in Figure 2b. Since the iodine of TBAI does not chemically bond to the sulfur defects of MoS₂, unlike 1.2-EDT in previous studies,^[10,14] it does not eliminate the depletion region of the MoS₂ FET. Rather, the transfer curve of Figure 2b shows n-type doping behavior of the MoS₂ FET through electron transfer from ZnS to MoS₂ during Fermi level equilibration (see Figure S3, Supporting Information). We note that transfer characteristics of the pristine MoS₂ FET and 2D-0D hybrid FET exhibited a similar transfer curve shape with only the threshold voltage shifted to the negative direction. This is because the capacitance of the h-BN gate dielectric layer in the two FETs is the same, while the QDs act as an n-type dopant and are not affected by the gate bias due to the thick tunneling barrier of ZnS. The transfer curve of the 2D-0D hybrid FET with h-BN exhibits gate hysteresis under $\Delta V_{\rm C} = 0.3$ V, and thus the minority carrier trap induced by the gate electric field can generally be excluded.^[15] To demonstrate the MM characteristics of the device, a pulsed laser of 0.5 Hz (green line) was used to stimulate the 2D-0D hybrid FET. Figure 2c shows different time-resolved photocurrent behaviors between a pristine MoS₂ FET and the 2D-0D hybrid FET under 532 nm wavelength laser pulse for 1 s. We note that the energy of the 532 nm wavelength light can both excite MoS₂ and CdSe. The pristine MoS₂ produced a low photocurrent due to its high exciton binding energy, and when the laser was turned off, the photocurrent (black line) decreased immediately to the dark current level. On the other hand, by coupling MoS₂ with CdSe/ZnS QDs, the 2D–0D hybrid produced an increased photocurrent and maintained it even after the laser illumination. The re-dark current gap between the pristine MoS₂ and 2D-0D hybrid is induced by charge trapping. We note that the ZnS shells with 10 layers and 5 layers showed excellent OMM and optical memory pixel (OMP) effects (Figure S6-3,a,b, Supporting Information), with the ten-layer ZnS shell showing a four times higher optically trapped current (OTC) than the five-layer ZnS shell. While the two-layer ZnS shell had adequate OTC at the vertical 2D-0D interface, leakage currents were present between lateral QDs, and this caused the OMP effect to disappear rapidly. To demonstrate critical repeatability such as programming and erasing, we designed a reset protocol of the trapped charge in which electrons from MoS₂ are transferred back to





Figure 2. 2D–0D hybrid device fabrication and OMM characteristics. a) Optical microscope images of the pristine MoS_2 FET and 2D–0D hybrid FET with a bottom electrode (black), h-BN dielectric layer (white), MoS_2 channel (violet), and CdSe/ZnS QDs (yellow). b) Transfer curves of the pristine MoS_2 and 2D–0D hybrid devices. c) Time-resolved photocurrent in the 2D FET ($V_D = 1 V$ and $V_G = -0.5 V$) and 2D–0D hybrid ($V_D = 1 V$ and $V_G = -2.5 V$) under 532 nm pulsed laser for 1 s. Schematic of the electron-trapping (programming) and electron-releasing (erasing) process between MoS_2 and a CdSe/ZnS QD by laser pulse and gate bias, respectively. d) Plot of the time-resolved current behavior under the same bias condition and laser pulses. Insets in each region illustrate the electron (blue)-hole (red) state of the conduction band (CB) and valance band (VB) in CdSe. A linear optically trapped current (OTC) defines the linear region ($N_{exciton} < N_{electron-VB}$), a shrunken OTC defines the saturated region ($N_{exciton} \geq N_{electron-VB}$). e) OTC behavior as a function of the number of pulses. The slopes denote the increments of current per optical pulse for the linear (green line), saturated (blue line), and occupied (black line) regions, which were extracted as 0.14, 0.06, and 0.02 μ A per optical pulse, respectively.

the CdSe core using a gate voltage pulse (Figure 2c schematic; Figure S3, Supporting Information). Figure 2d illustrates such a MM function with three distinct regions under the multi-pulsed laser of 0.5 Hz. In the first region, or linear region, OTC is linearly stacked according to the number of laser pulse exposures. In this linear region, the number of excitons (N_{exciton}) generated in the CdSe/ZnS QDs should be less than the number of electrons in the valence band ($N_{\text{electron-VB}}$). Then the CdSe can linearly trap the photogenerated holes of the generated excitons. Because photogenerated electrons move from CdSe to MoS₂ via tunneling, not 100% of the electrons but rather only an exponentially reduced number of electrons are transferred. The residual electrons in the CdSe core recombine with the holes and cancel the hole trapping effect. In the second region, or saturated region, as $N_{\rm exciton}$ becomes similar to or less than $N_{\rm electron-VB}$, the OTC begins to slowly decrease. Finally, in the third region, or hole-occupied region, since $N_{\text{electron-VB}}$ is almost depleted and the CdSe core is not able to generate excitons, the additional hole

trap is also limited. The memory state retention stability was >70 s in the linear region, as detailed in Figure S4 (Supporting Information). During measurement, we utilized an optimized condition of gate voltage as -2.5 V for electron depleted condition that is confirmed in Figure S5-2 (Supporting Information). For a comprehensive understanding, we present the OTC behavior in terms of the threshold voltage (V_{th}) shift of the transfer curves induced by optical pulses (see Figure S5-3, Supporting Information). Figure 2e summarizes the OTC as a function of the number of laser pulses. The slopes represent the increments of current per optical pulse for the linear (green line), saturated (blue line), and occupied (black line) regions, which were extracted as 0.14, 0.06, and 0.02 µA per optical pulse, respectively. Converting the total current increased by the OMM effect to gate bias gives a difference of $\Delta V_{\rm G}$ = 0.4 V, from $V_{\rm G}$ = -2.45 V to $V_{\rm G}$ = -2.05 V, and the charge concentration change is calculated as 1.2×10^{11} cm⁻³ (see Figure S5-1, Supporting Information). In principle, the decaying current and slightly increased re-dark current observed in







Figure 3. Optically trapped current mechanism and memory pixel effect according to laser pulse exposure position. a) Schematic description of the band alignment of MoS_2 and CdSe/ZnS (blue and red colors denote the conduction band and valence band, respectively), charge transfer, and trap mechanism. b) OTC behavior in the linear, saturated, and occupied regions. Each straight colored line (green, blue, and black) indicates the slope of the current level accumulated by the OMM. c) Positions and scanning direction of the laser pulses labeled as zones 1, 2, and 3. d) Equivalent circuit by a parallel connection of variable resistors ($R_{MoS2} - R_{photo}$). R_{photo} is a constant resistance reduced by laser pulses. e) OMM characteristics ($V_D = 1$ V and $V_G = -2.5$ V) according to focused laser pulses in different zones.

the pristine MoS₂ device can be explained by the persistent photoconductivity (PPC) effect in TMD materials including MoS₂, which originates from intrinsic chalcogenide defects in TMDs or extrinsic defects at the TMD/substrate interface.[16-18] In our study, we utilized an h-BN layer as the substrate, which is known for its defect-free interface with van der Waals (vdW) materials such as MoS₂. Therefore, we propose that the PPC in our device originates from sulfur vacancies within the MoS₂ channel. Conversely, the increased current observed in the 2D-0D hybrid device is likely attributed to the presence of shallow traps that are activated by the gate voltage applied from the bottom electrode. These shallow traps may form at the interface between MoS₂ and ZnS or arise from absorbates originating from the solvent of the QDs solution. Upon applying an optical pulse under a gate voltage of -2.5 V (electron-depleted condition within the channel) to the 2D-0D hybrid device, it is plausible that electrons from the shallow traps are injected into the MoS₂ channel, resulting in an enhanced channel conductance and subsequently increased current within the device. Although the increase in current from electrons injected into the channel from shallow traps is much smaller compared to that from QDs, mitigation would be a further challenge. One possible means might be treatment with a solution to passivate the shallow traps in our device, or otherwise mitigate the aging process.

2.3. Optically Trapped Current Mechanism

Figure 3a depicts band diagrams of three different states of the 2D-0D hybrid OMM device: equilibrium, illumination, and postillumination states. In the equilibrium state, MoS₂ and CdSe are isolated by the high barrier of the ZnS shells, of which the bandgap is 3.54 eV.^[19] In the illumination state, the barrier allows electron transfer from CdSe to MoS₂ through tunneling and rectifies the reverse thermionic electron transfer from MoS₂ to the CdSe cores. The ZnS shells also allow the holes in the CdSe cores to maintain a stable trap under n-doping $V_{\rm G}$ conditions, where the Fermi level of MoS₂ is higher than the Fermi level of CdSe (see Figure S5-1, Supporting Information). Immediately after illumination, the photocurrent presents a sharp horn shape in the plots (black circles in Figure 3b) because the trap effect is momentarily attenuated by the decay current of MoS₂ and the recombination of the residual charge in the CdSe/ZnS QDs. The holes trapped in the CdSe cores push down the Femi level toward the valance band and induce electrostatic doping in the MoS₂ channel due to the Fermi level difference ($V_{\rm 2D-0D gate}$) between MoS₂ and CdSe. As a result, electrons accumulate on the top side of the MoS₂ channel adjacent to CdSe/ZnS QDs according to the number of pulsed lasers (violet dashed lines in Figure 3a), which generates OTC current. Figure 3b provides a detailed look into



the distinct behaviors of the three regions introduced in the previous section. In the linear region (green line) and saturated region (blue line), the OTC remains stable (gray dashed line) after the laser pulses. But in the saturated region, the OTC starts to gradually decrease as a function of the number of laser pulses. Finally, in the occupied region (black line), the OTC disappears and accordingly, the memory stability collapses (gray dashed line). We estimate that the dominant origin of the fast-decaying characteristic in the sharp horn shape is not the continuous backflow of electrons to the CdSe core, but rather the persistent photoconductivity (PPC) effect or the recombination of photocarriers generated in MoS₂.^[16–18] The only difference in the current behavior between linear and occupied regions is that in the occupied region, the QDs no longer function as charge traps, and therefore the current behavior is dominated by the PPC effect or recombination in MoS₂.

2.4. Optical Memory Pixel Effect of the QD Matrix

According to the device design, there is one ZnS shell between the QDs and MoS₂ but there is a double ZnS shell between the QDs in the CdSe/ZnS matrix, and thus the probability of charge transport between QDs is reduced exponentially according to the tunneling possibility theory, that is, they are basically isolated (see Figure S6-1, S6-2, Supporting Information). To prove that only QDs exposed to laser pulses show memory properties, we designed a map of focused laser positions (wavelength = 532 nm, beam size <1 µm) and scanned from left to right; the three different positions are referred to as zone 1, 2, and 3, as shown in Figure 3c. Each of the three zones can be expressed as an equivalent circuit by a parallel connection (R_{MoS2}) of variable resistors, as shown in Figure 3d. In addition, the CdSe/ZnS QDs composite has limitations in OTC, so it is assumed to have a constant $-R_{\rm photo}$. As a result, Figure 3e reveals both OMM and OMP effects as a function of exposure position. The 2D-0D hybrid OMM device maintained a consistent OTC during exposure to 8 to 10 pulses before moving to the occupied region, and therefore $R_{\rm photo}$ (15.35 M Ω) can be determined based on the OTC value modulated by the OMM effect in zone 1 (red-shaded area in Figure 3e). The laser scanning system then stimulated zone 2 and zone 3 according to the exposure position of the laser pulse. Even at the different positions, the results repeatedly showed stable OMM characteristics. However, the magnitude of the current increase in zone 1 gradually decreases toward zone 2 and zone 3. From the point of view of the equivalent circuit, we theoretically calculated the $R_{\rm photo}$ in zones 1, 2, and 3. If the calculated $R_{\rm photo}$ is assumed to be constant, the calculated OMP trend is consistent with the real OMP trend (see Figure S7, Supporting Information). As a result, the observed OMP effect proved that each QD could have a different memory state without current leakage between the QDs. Additional 2D-0D hybrid OMM devices consistently showed reliable and repeatable results (see Figure S8, Supporting Information).

2.5. Fully Laser-Pulse-Operated Multi-Level Memory Inverter

As above, the 2D–0D hybrid OMM device was able to exhibit multi-level programming characteristics by inducing an OTC,

but realizing a linearly optical erasing process was impossible. To further explore this point, based on the OMP effect of the QD matrix demonstrated in Figure 3e, we designed an inverter that can perform the erasing function with laser pulses. As shown in Figure 4a, the proposed inverter consists of two 2D-0D hybrid OMM devices connected in series. Here, because each QD in the entire 2D–0D hybrid structure is a floating gate memory unit, the spot size of the finely focused laser beam can be assigned as an OMM unit device, which is $<1 \mu m$ in this case. Then, the row of scanning laser pulses becomes one MM inverter. To demonstrate the operation of five independent MM inverters in one 2D-0D hybrid structure, we designed the pathway of the scanning laser pulses to pass through five rows, as shown in Figure 4b. The fabricated device has a short channel length of 3 µm and a wide width of 10 µm (programming is denoted as the blue line, and erasing as the red line), and thus it is optimized to stimulate the focused laser along each row (black dashed line in Figure 4c). Figure 4d shows five repeated MM functions with 532 nm laser pulses of 0.5 Hz, demonstrating that both highly linear programming and erasing processes were conducted solely with laser pulses of the same wavelength. We note that while some previous OMM devices have demonstrated potentiation characteristics with optical pulses, they adopted electrical means or different wavelengths of optical pulses to demonstrate depression characteristics (see Table S1, Supporting Information). To the best of our knowledge, a strategy to achieve both potentiation and depression using optical pulses with the same wavelength has not been reported yet. Results confirmed that the QDs exposed to the laser pulses have independent memory characteristics. This result is believed to represent an important flag in the QD memory field and furthermore can greatly contribute to the expansion of ultra-simple memory device fabrication using QD lithography.^[20] During measurement, the slope of the increase in output voltage differed for the five rows. We estimate the reasons for this to be the nonuniform bonding interface between QDs and MoS₂ and the precise location of the focused 532 nm laser (see Figure S11, Supporting Information).

2.6. Training and Inference Task using CIFAR-10 Dataset

Finally, we tested the applicability of the OMM inverters to act as synapses in a hardware-neural network (HW-NN) with a training task for recognition using the CIFAR-10 dataset. Adopting the DNN+NeuroSim V2.1 benchmarking framework, a HW-NN comprising OMM inverter synapses was trained and inferenced based on the VGGNet model consisting of an eight-layered convolution neural network (CNN) and then evaluated through the CIFAR-10 dataset (containing images of, for example, a dog, horse, truck, and so on).^[21] Figure 5a shows the HW-NN structure for matrix-vector multiplication comprising the OMM inverter synapses, which are applicable to the implementation of the fully connected layers within the CNN. Here, we introduced converting resistances (R_{conv}) to each OMM inverter to convert the output voltage (V_{out}) to current (I_{conv}). The conductance of the OMM inverters is then determined as $W = I_{conv}/V_{in}$ = $(V_{\rm out}/R_{\rm conv})/V_{\rm in}$. A detailed description of the conductance of the OMM inverters is provided in Figure S9 (Supporting

IENCE NEWS



Figure 4. Fully laser-pulse-operated OMM inverter. a) Schematic diagram of the OMM inverter consisting of two 2D–0D hybrid memory devices connected in series and driven by the law of voltage division. One device conducts programming (blue) and the other conducts erasing (red) according to scanning laser pulses. b) Equivalent memory circuit model according to the laser pulse exposure positions. The laser scan over five rows induces five independent inverter characteristics. c) Optical microscope image of the 2D–0D hybrid OMM inverter. The blue and red rectangular boxes indicate the programming and erasing operations. Scale bar is 3 μ m. d) Plot of multi-level memory inverter characteristics ($V_D = 1$ V and $V_G = -3$ V) according to the laser pulse exposure positions.

Information). A pair of equivalent OMM inverters is adopted to represent both positive and negative synaptic weight values. In this structure, the synaptic weight is determined as a subtraction of the conductance of the OMM inverters designed for positive and negative weights $(W = W_{\rm p} - W_{\rm N})$.^[21] Our synaptic cell is composed of four optically controllable devices, where two devices are for potentiation ($\delta W_{\rm cell} >$ 0) and two devices are for depression (δW_{cell} < 0). Therefore, a hardware-based bidirectional weight update scheme that updates the OMM inverter designed for a positive/negative synaptic weight when the weight is in the positive/negative weight range (see Figure 5b) can be adopted for low power consumption in our architecture.^[22] We extracted a nonlinear value for five OMM inverters (see Figure 5c), where the nonlinearity for potentiation was in the range from 1.24 to 1.54 and the nonlinearity for depression was in the range from -1.14 to -0.62. The behavioral model for nonlinearity extraction is provided in Figure S10 (Supporting Information).^[21] Finally, we emulated the recognition rates of the HW-NN composed of the OMM inverters for the CIFAR-10 dataset consisting of 50 000 training and 10 000 inference datasets for each epoch. The recognition accuracy exhibited a gradual increase as the number of training epochs progressed, and we observed an abrupt increase in accuracy after the 200th training epoch. This change is attributed to the fine-tuning of the learning rate, which is implemented in Neurosim+ to promote efficient convergence of accuracy.^[21] As a result, the highest maximum recognition rate was confirmed as 91% (see Figure 5d). The high recognition rate achieved by our OMM inverter-based synaptic devices originates from the utilization of only the linear region of the independent memory characteristics of the QDs (see Table S1, Supporting Information). Detailed simulation conditions are provided in Table S2 (Supporting Information).

3. Conclusion

We fabricated an OMM device within a MoS₂ FET using CdSe/ZnS type-I core/shell QDs. In this design, the thickness of the ZnS shell is important to characterize the memory. The mechanism driving the OMM characteristics was identified as three different operating regions, namely linear, saturated, and occupied regions. It was found that a strong gate voltage pulse can reset the memory, thereby paving the way toward repetitive MM operation. However, since this does not achieve full OMM, by employing the voltage division effect of inverters, we demonstrated a 2D-0D hybrid inverter that performs both programming and erasing operations with laser pulses only. Finely focused laser scanning confirmed that the QDs in the hybrid inverter can act as a floating gate memory unit because the sufficiently thick ZnS shell prevents charge leakage between QDs. Based on this electrically isolated QD architecture, we devised a laser pulse scan that passes through five rows in the 2D-0D hybrid structure and realized five different OMM characteristics at once. Finally, a fully optically-controlled intelligent system based on OMM inverters achieved a high maximum recognition rate of 91% in a CIFAR-10 pattern recognition task using a CNN.

www.advmat.de

ADVANCED SCIENCE NEWS



Figure 5. CIFAR-10 dataset recognition task. a) Hardware-neural network comprising fully optically-controlled inverters for the fully connected layers. b) Hardware-based bidirectional weight update scheme. Each OMM inverter has a blue and a red resistor, which are variable resistors for potentiation and depression, respectively. Two inverters form a unit synaptic cell. c) Nonlinearity of the potentiation and depression curve of the five inverters. d) Recognition rate of the five inverters for the CIFAR-10 dataset.

S

www.advmat.de

ADVANCED SCIENCE NEWS

www.advancedsciencenews.com

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

H.-S.R., T.W.K., and D.A.T. contributed equally to this work. D.K. Hwang acknowledges financial support from the Korea Institute of Science and Technology (KIST) Institution Program (grant no. 2E32242), KU-KIST School project, the National Research Foundation of Korea (NRF) (grant no. 2023R1A2C2003985), and the Institute for Information & Communications Technology Promotion (IITP) (grant. no. 2020-00841). J.S.L. acknowledges financial support from the National Research Foundation of Korea (NRF) grant (2022R1A2C2008278) and the DGIST R&D Program (grant no. 23-CoE-NT-01 and no. 23–SENS2–3) funded by the Korean government (MSIT).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

2D-0D hybrid, inverters, optical multi-level memory, recognition task

Received: April 19, 2023

- Revised: July 14, 2023 Published online: July 27, 2023
- a) J. W. Jeong, Y.-E. Choi, W.-S. Kim, J.-H. Park, S. Kim, S. Shin, K. Lee, J. Chang, S.-J. Kim, K. R. Kim, *Nat. Electron.* **2019**, *2*, 307; b) H. Yoo, H. Park, S. Yoo, S. On, H. Seong, S. G. Im, J. J. Kim, *Nat. Com*-
- Yoo, H. Park, S. Yoo, S. On, H. Seong, S. G. Im, J. J. Kim, Nat. Commun. 2019, 10, 2424; c) M. Andreev, S. Seo, K. S. Jung, J. H. Park, Adv. Mater. 2022, 34, 2108830; d) S. S. Kim, S. K. Yong, W. Kim, S. Kang, H. W. Park, K. J. Yoon, D. S. Sheen, S. Lee, C. S. Hwang, Adv. Mater. 2022, https://doi.org/10.1002/adma.202200659. e) K. Kobashi, R. Hayakawa, T. Chikyow, Y. Wakayama, Nano Lett. 2018, 18, 4355; f) M. Andreev, J. W. Choi, J. Koo, H. Kim, S. Jung, K. H. Kim, J. H. Park, Nanoscale Horiz. 2020, 5, 1378; g) J. Shim, S. Oh, D. H. Kang, S. H. Jo, M. H. Ali, W. Y. Choi, K. Heo, J. Jeon, S. Lee, M. Kim, Y. J. Song, J. H. Park, Nat. Commun. 2016, 7, 13413; h) V. K. Sangwan, H. S. Lee, H. Bergeron, I. Balla, M. E. Beck, K. S. Chen, M. C. Hersam, Nature 2018, 554, 500; i) S. Seo, J. Koo, J.-W. Choi, K. Heo, M. Andreev, J.-J. Lee, J.-H. Lee, J.-I. Cho, H. Kim, G. Yoo, D.-H. Kang, J. Shim, J.-H. Park, npj 2D Mater. Appl. 2021, 5, 32.

and Conditions

(https://onlinelibrary.wiley

and

conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Common

www.advmat.de

- [2] S. Seo, J. I. Cho, K. S. Jung, M. Andreev, J. H. Lee, H. Ahn, S. Jung, T. Lee, B. Kim, S. Lee, J. Kang, K. B. Lee, H. J. Lee, K. S. Kim, G. Y. Yeom, K. Heo, J. H. Park, *Adv. Mater.* **2022**, *34*, 2202799.
- [3] a) S. M. Hus, R. Ge, P. A. Chen, L. Liang, G. E. Donnelly, W. Ko, F. Huang, M. H. Chiang, A. P. Li, D. Akinwande, *Nat. Nanotechnol.* **2021**, *16*, 58; b) M. Lee, W. Lee, S. Choi, J. W. Jo, J. Kim, S. K. Park, Y. H. Kim, *Adv. Mater.* **2017**, *29*, 1700951; c) S. Seo, S. H. Jo, S. Kim, J. Shim, S. Oh, J. H. Kim, K. Heo, J. W. Choi, C. Choi, S. Oh, D. Kuzum, H. P. Wong, J. H. Park, *Nat. Commun.* **2018**, *9*, 5106.
- [4] R. Xu, H. Jang, M. H. Lee, D. Amanov, Y. Cho, H. Kim, S. Park, H. J. Shin, D. Ham, *Nano Lett.* **2019**, *19*, 2411.
- [5] a) Z. Zhu, M. Janasik, A. Fyffe, D. Hay, Y. Zhou, B. Kantor, T. Winder, R. W. Boyd, G. Leuchs, Z. Shi, *Nat. Commun.* 2021, *12*, 1666; b) L. Li, D. Wang, D. Zhang, W. Ran, Y. Yan, Z. Li, L. Wang, G. Shen, *Adv. Funct. Mater.* 2021, *31*, 2104782; c) L. Mennel, J. Symonowicz, S. Wachter, D. K. Polyushkin, A. J. Molina-Mendoza, T. Mueller, *Nature* 2020, *579*, 62.
- [6] D. Jariwala, T. J. Marks, M. C. Hersam, Nat. Mater. 2017, 16, 170.
- [7] a) Y. Sun, Y. Ding, D. Xie, J. Xu, M. Sun, P. Yang, Y. Zhang, *Opt. Lett.* **2021**, 46, 1748; b) Q. Wang, Y. Wen, K. Cai, R. Cheng, L. Yin, Y. Zhang,
 J. Li, Z. Wang, F. Wang, F. Wang, T. A. Shifa, C. Jiang, H. Yang, J. He,
 Sci. Adv. **2018**, *4*, 7916.
- [8] a) E. Zhang, W. Wang, C. Zhang, Y. Jin, G. Zhu, Q. Sun, D. W.
 Zhang, P. Zhou, F. Xiu, ACS Nano 2015, 9, 612; b) S. Bertolazzi;, D.
 Krasnozhon;, A. Kis;, ACS Nano 2013, 7, 3246.
- [9] J. Lim, B. G. Jeong, M. Park, J. K. Kim, J. M. Pietryga, Y. S. Park, V. I. Klimov, C. Lee, D. C. Lee, W. K. Bae, Adv. Mater. 2014, 26, 8034.
- [10] H. S. Ra, D. H. Kwak, J. S. Lee, Nanoscale 2016, 8, 17223.
- [11] G. Konstantatos, M. Badioli, L. Gaudreau, J. Osmond, M. Bernechea, F. P. Garcia de Arquer, F. Gatti, F. H. Koppens, *Nat. Nanotechnol.* 2012, 7, 363.
- [12] K. F. Mak, C. Lee, J. Hone, J. Shan, T. F. Heinz, Phys. Rev. Lett. 2010, 105, 136805.
- [13] H. S. Ra, A. Y. Lee, D. H. Kwak, M. H. Jeong, J. S. Lee, ACS Appl. Mater. Interfaces 2018, 10, 925.
- [14] D. Kufer, I. Nikitskiy, T. Lasanta, G. Navickaite, F. H. Koppens, G. Konstantatos, Adv. Mater. 2015, 27, 176.
- [15] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage Jr., S. J. Kim, B. Kippelen, Adv. Mater. 2011, 23, 1293.
- [16] P. Ci, X. Tian, J. Kang, A. Salazar, K. Eriguchi, S. Warkander, K. Tang, J. Liu, Y. Chen, S. Tongay, W. Walukiewicz, J. Miao, O. Dubon, J. Wu, *Nat. Commun.* 2020, *11*, 5373.
- [17] S. Chandan, S. Sarkar, B. Angadi, Appl. Phys. Lett. 2021, 118, 172105.
- [18] S. Seo, J.-J. Lee, R.-G. Lee, H. Kim, S. Park, S. Jung, H.-K. Lee, M. Andreev, K.-B. Lee, K.-S. Jung, S. Oh, H.-J. Lee, K. S. Kim, Y. Yeom, Y.-H. Kim, J.-H. Park, *Adv. Mater.* **2021**, *33*, 2102980.
- [19] X. Wang, J. Yu, R. Chen, Sci. Rep. 2018, 8, 17323.
- [20] S. Myeong, B. Chon, S. Kumar, H. J. Son, S. O. Kang, S. Seo, Nanoscale Adv. 2022, 4, 1080.
- [21] X. Peng, S. Huang, H. Jiang, A. Lu, S. Yu, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 2021, 40, 2306.
- [22] S. Lim, J.-H. Bae, J.-H. Eum, S. Lee, C.-H. Kim, D. Kwon, B.-G. Park, J.-H. Lee, Neural Comput. Appl. 2018, 31, 8101.