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Hole Current Enhancement Using $W_{1-x}Cr_xSe_2$ Alloy Interface for p-Type WSe_2 FETs

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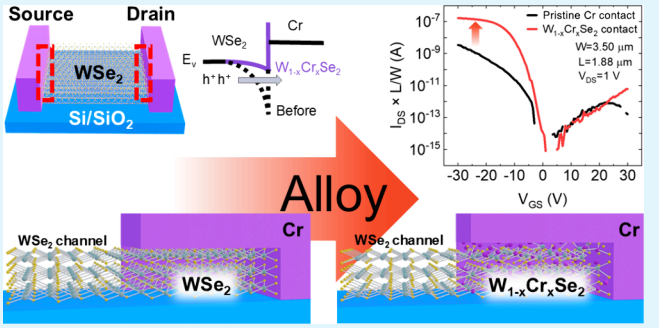
ABSTRACT: Two-dimensional (2D) transition-metal dichalcogenides (TMDs) have emerged as promising candidates for next-generation semiconductor devices. Among TMDs, tungsten diselenide (WSe_2) is regarded as an ideal material for p-type field-effect transistors (FETs). However, the realization of high-performance p-type devices remains limited due to undesired ambipolar behavior and high contact resistance. These challenges originate from Fermi level pinning (FLP) caused during conventional deposition processes. Although van der Waals (vdW) contacts have been introduced to overcome FLP, their implementation faces difficulties due to contamination-induced degradation and limitations in CMOS process compatibility. In this study, we demonstrate a scalable approach for p-type contact via the $W_{1-x}Cr_xSe_2$ alloy interface. It has been reported that Cr incorporation reduces the bandgap of WSe_2, while Cr_xSe_y exhibits p-type semimetal properties. Leveraging these properties, thermal annealing of Cr contacts enables the formation of $WSe_2/W_{1-x}Cr_xSe_2/Cr$ layers at the contact region. This interfacial alloy effectively suppresses FLP, eliminates undesirable ambipolar behavior, and enhances hole injection. The resulting devices achieve a Schottky barrier height as low as 61.1 meV and reduce contact resistance by approximately 3 orders of magnitude. Consequently, $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs exhibit robust p-type performance with an average on/off current ratio of 2.19×10^8 across 20 devices. These findings present a practical and scalable strategy for engineering low-resistance p-type contacts in WSe_2, providing an important step toward the integration of TMD-based complementary logic in future scaled CMOS technologies.



KEYWORDS: *2D materials, WSe_2, Schottky barrier, contact, alloy interface*

INTRODUCTION

Transition-metal dichalcogenides (TMDs) have attracted considerable attention as promising materials for next-generation semiconductor devices due to their atomically thin structure and excellent electrical properties. These properties of TMDs enable effective suppression of short-channel effects, and their dangling-bond-free structures minimize mobility degradation from surface roughness scattering in ultrascaled devices.[1,2] Therefore, investigating TMD materials is essential for future device scaling. MoS_2, a representative n-type TMD, shows great promise for next-generation NMOS owing to its high mobility and stability.[3,4] However, the development of p-type TMDs has been relatively slow. Among various p-type TMDs, tungsten-diselenide (WSe_2) stands out as an ideal candidate for p-type field effect transistors (FETs) because of its suitable energy band structure.[5−8] Research on doping approaches such as WO_x and MoO_x has enhanced the p-type properties of WSe_2, although challenges such as reproducibility still need to be addressed.[9−11] Also, most metal electrodes form a high Schottky barrier when interfaced with p-type TMDs, leading to poor hole injection efficiency.[12] Moreover, the choice of metals for p-type contacts is even more limited compared to n-type contacts. Consequently, compared to n-type TMDs, the progress of p-type TMDs remains insufficient. Since the performance of NMOS and PMOS must be balanced for next-generation CMOS applications, further efforts are required to improve the p-type characteristics of WSe_2.

A key challenge to achieving high-performance WSe_2 FETs is the reduction of contact resistance. However, achieving low-resistance p-type contacts is difficult due to Fermi level pinning (FLP).[13,14] FLP prevents the metal−semiconductor junction from following the ideal Schottky−Mott rule, leading to inefficient hole injection and undesired n-type or ambipolar behavior, thereby limiting device performance. This issue mainly arises from damage to the TMD structure caused during metal deposition, leading to severe metal-induced gap

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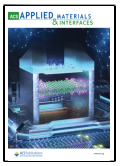

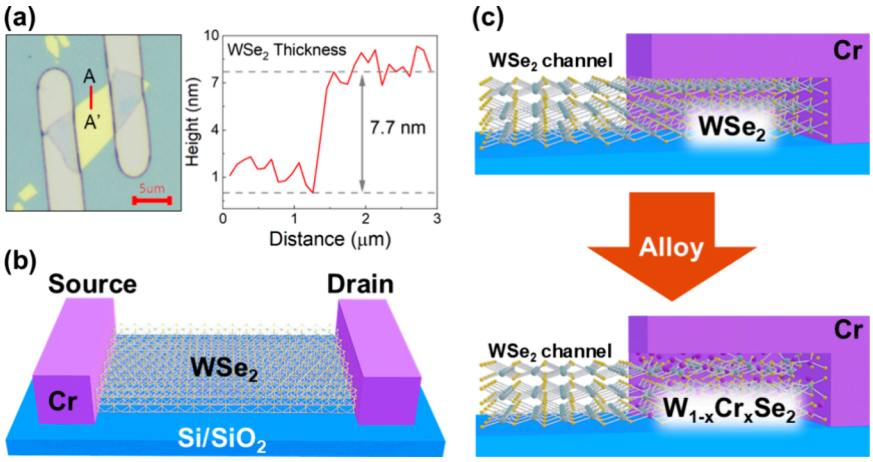

Figure 1. Schematics of WSe_2 FETs with a $W_{1-x}Cr_xSe_2$ alloy interface. (a) Optical microscopy image of the WSe_2 FET and the thickness of the WSe_2 channel measured along A−A′. The thickness of the WSe_2 flake was measured by atomic force microscopy (AFM), and the flake used in the device was 7.7 nm thick (~11 layers). (b) Schematic structure of the WSe_2 FET. (c) Comparison of the structures at the source/drain regions before and after the formation of the $W_{1-x}Cr_xSe_2$ interface between Cr and WSe_2.

states (MIGS). Such damage occurs in conventional deposition processes (e.g., evaporation or sputtering), where high-energy metal atoms strike the TMD surface.[15,16]

To overcome this issue, van der Waals (vdW) contacts have recently been proposed, offering atomically clean interfaces that can effectively suppress FLP.[17] vdW contacts have been developed as a low-energy process that does not cause damage to the surface of TMDs. vdW contacts utilizing low melting point metals or buffer layers have been actively investigated to reduce interfacial disorder.[18−21] However, these metals typically have low work functions, which makes them unsuitable for p-type transistors that require efficient hole injection. Also, the buffer layer or its residuals may hinder contact optimization. Another typically involves forming the contact material in advance, followed by its physical transfer onto the surface of TMDs. This approach has prompted significant research into materials appropriate for p-type transistors.[22−25] However, many of these materials cannot be directly deposited, and the transfer process is prone to contamination, posing significant challenges for practical implementation.[26] In addition, the vdW gap can lead to parasitic components and increased contact resistance in short-channel devices.[27−30] That is, although vdW contacts provide an effective means of engineering device polarity, they also suffer from process-related limitations and drawbacks associated with the vdW gap. The ultimate goal for WSe_2 FETs is to simultaneously achieve robust p-type operation and low contact resistance. Furthermore, to fulfill their potential as channel materials for next-generation scaled devices, they must be compatible with industrially relevant wafer-scale processes.

In this work, we demonstrate the direct formation of an interfacial layer for p-type contact through $W_{1-x}Cr_xSe_2$ alloy interface. It has been reported that Cr can reduce the bandgap when incorporated into the WSe_2 lattice.[31] In addition, Cr_xSe_y is known to exhibit p-type semimetal characteristics.[32] Based on these properties, the p-type characteristics of WSe_2 are expected to be enhanced. Furthermore, when Cr is used as a contact metal for WSe_2, thermal annealing enables the facile formation of $WSe_2/W_{1-x}Cr_xSe_2/Cr$ layers only in the source/drain regions. The present work confirms that the $W_{1-x}Cr_xSe_2$ alloy interface disregards FLP and eliminates undesirable ambipolar behavior, thereby enabling robust p-type operation. This alloying effectively lowers the Schottky barrier height (SBH) to 61.1 meV and significantly reduces the contact resistance by approximately 3 orders of magnitude. As a result, the $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs exhibit high-performance p-type operations, achieving an average on/off ratio of 2.19×10^8 across 20 devices. This approach provides a practical and scalable route to optimize contact properties, overcoming limitations for device scaling.

EXPERIMENTAL SECTION

Device Fabrication. Multilayer WSe_2 (HQ Graphene) was mechanically exfoliated onto a SiO_2 (200 nm)/P^{2+} Si substrate using the Scotch tape method via a dry transfer process. GXR-601 (positive photoresist) was spin coated at 1500 rpm, followed by a soft bake. The 532 nm continuous wave laser was used to pattern the source/drain regions. Cr (35 nm) was deposited by thermal evaporation, and the electrodes were formed using a lift-off process with acetone, followed by rinsing with IPA and DI water.

$W_{1-x}Cr_xSe_2$ Alloy Formation. Cr films (35 nm) were deposited by thermal evaporation onto the WSe_2, followed by rapid thermal processing at 500 °C for 2 min under a low-vacuum condition (~400 mTorr) in an Ar atmosphere to form the $W_{1-x}Cr_xSe_2$ alloy interface.

Characterizations. The chemical composition of the samples was analyzed using Raman spectroscopy and X-ray photoelectron spectroscopy. Electrical characteristics of the WSe_2 FETs were measured under ambient conditions using a Keithley 4200A-SCS semiconductor parameter analyzer. The Schottky barrier height was extracted based on the thermionic emission model from temperature-dependent transfer characteristics. Temperature-dependent transfer characteristics were measured under high vacuum using liquid nitrogen.

RESULTS AND DISCUSSION

Figures 1(a) and 1(b) show the back-gate WSe_2 FETs. The detailed fabrication process is described in Figure S1. It has been reported that mobility is higher in three or more layers compared to monolayers, and ambipolar behavior can be observed up to a thickness of 5−15 nm.[6,33] In addition, few-layer or thicker WSe_2 shows reduced variations in electrical properties caused by ambient adsorbates compared to monolayers.[34] Furthermore, since the formation of an alloy layer with Cr requires enough Se atoms, a multilayer WSe_2 with an appropriate thickness is necessary for this study.

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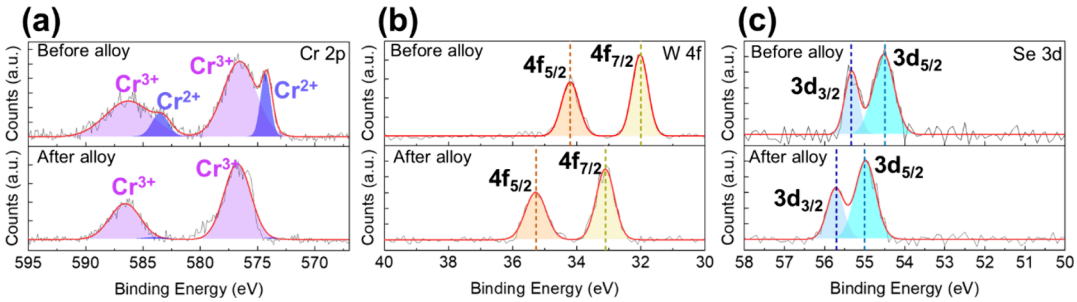

Figure 2. XPS analysis results before and after alloying between Cr and WSe_2. (a) Cr 2p spectra showing characteristic peaks corresponding to Cr^{2+} and Cr^{3+} oxidation states. (b) W 4f spectra and (c) Se 3d spectra confirming binding energy shift after alloying.

Cr is employed as a contact metal for WSe_2 to facilitate the formation of a $WSe_2/W_{1-x}Cr_xSe_2/Cr$ layers at the source/drain regions, which enhances p-type characteristics by suppressing ambipolar behavior and enabling stable, efficient hole injection. To form the $W_{1-x}Cr_xSe_2$ alloy interface in the fabricated device, Rapid Thermal Process (RTP) was employed. During RTP, Cr atoms thermally diffuse toward the WSe_2, resulting in the formation of the $W_{1-x}Cr_xSe_2$ alloy interface, Figure 1(c). Since $W_{1-x}Cr_xSe_2$ is formed in the Cr−WSe_2 interface, the WSe_2 channel remains undamaged.[35,36]

If RTP is performed in ambient air, WO_x may form on the WSe_2 channel. Because WO_x acts as a p-type doping for WSe_2, this effect must be carefully controlled.[10,11,37,38] To eliminate the possibility of unintended p-type doping by WO_x, all experiments were conducted under an Ar atmosphere at a pressure of approximately 400 mTorr. To identify the optimal temperature for forming the alloy, the RTP was carried out at various temperatures ranging from 200 to 600 °C for a fixed duration of 2 min (Figure S4). As a result, it was determined that 500 °C is the optimal temperature condition for the formation of the $W_{1-x}Cr_xSe_2$ alloy interface.

X-ray photoelectron spectroscopy (XPS) was conducted to confirm the formation of the $W_{1-x}Cr_xSe_2$ alloy interface after RTP. The atomic composition was calculated to be W 18.42%, Cr 21.85%, and Se 59.73%. Therefore, based on the metal atom ratio, the composition can be expressed as $W_{1-x}Cr_xSe_2$ with $x = 0.54$. As shown in Figure 2(b), WO_x-related peaks were absent in the W 4f spectrum, indicating that the influence of WO_x has been effectively suppressed. (WO_x signals are typically detected around ∼36 eV and ∼38 eV).[11,39]

Figure 2(a) presents the Cr 2p spectrum, demonstrating the formation of $W_{1-x}Cr_xSe_2$ after RTP under an Ar atmosphere. The Cr 2p states generally appear at different binding energies (B.E.) depending on their oxidation states. Before alloying, peaks corresponding to both Cr^{2+} and Cr^{3+} are observed (574.2 and 583.4 eV for Cr^{2+}, 576.7 and 586.4 eV for Cr^{3+}[40]). After alloying, the Cr^{2+} peaks are nearly eliminated, and the spectrum is dominated by Cr^{3+} peaks. This change in oxidation state suggests that Cr atoms have reacted with W and Se atoms.[32,41] Additionally, a blue shift in Cr-related Raman peaks was observed after alloying, as shown in Figure S2, supporting the chemical interaction between Cr and WSe_2.[40] Moreover, the E^1_{2g} and A_{1g} modes of WSe_2 remained nearly unchanged, indicating that its lattice structure was largely preserved.

Figures 2(b) and 2(c) show that the B.E. of the W 4f and Se 3d peaks shift to higher values after alloying. Specifically, the W 4f states shift by approximately 1 eV (32.01 and 34.2 eV before alloying corresponding to W $4f_{5/2}$ and W $4f_{7/2}$, respectively; 33.1 and 35.2 eV after alloying corresponding to W $4f_{5/2}$ and W $4f_{7/2}$, respectively), while the Se 3d states shift by about 0.4 eV (54.5 and 55.3 eV before alloying corresponding to Se $3d_{5/2}$ and Se $4f_{3/2}$, respectively; 54.9 and 55.7 eV after alloying corresponding to Se $3d_{5/2}$ and Se $4f_{3/2}$, respectively). An increase in B.E. is often interpreted as indicative of n-type doping. However, in this case, the observed peak shifts in W 4f and Se 3d are attributed to changes in the band structure rather than doping. It has been reported that the incorporation of Cr atoms into WSe_2 can induce new energy states below the conduction band minimum, effectively narrowing the bandgap. This phenomenon is attributed to the increased contribution of Cr d-orbitals in the conduction band.[31,42,43] Furthermore, the relatively low formation energy of Cr (∼0.7 eV) allows effective alloying with WSe_2 under low-temperature annealing.[31] As the value of x increases in $W_{1-x}Cr_xSe_2$, the bandgap is further reduced, and p-type metallic behavior is observed at $x = 1$.[32] The observed shifts in W 4f and Se 3d binding energies are consistent with previous reports and suggest the possibility of changing band structure at the Cr−WSe_2 interface. The $W_{1-x}Cr_xSe_2$ ($x = 0.54$) formed by RTP indicates that enough Cr reacted with WSe_2. This suggests that the $W_{1-x}Cr_xSe_2$ likely possesses a sufficiently narrower band structure than WSe_2, with multiple energy states existing below the conduction band minimum. This implies that the $W_{1-x}Cr_xSe_2$ can withdraw electrons from WSe_2, leading to a possible charge transfer at the interface.

Furthermore, only the Cr^{3+} peak remains after the formation of the $W_{1-x}Cr_xSe_2$ alloy interface. In pristine WSe_2, W and Se exist predominantly as W^{4+} and Se^{2-}, respectively. The substitution of Cr^{3+} for W^{4+} in pristine WSe_2 can be regarded as a form of hole doping. However, typical doping processes introduce donor or acceptor levels without significantly altering the intrinsic bandgap of the pristine material. In contrast, when Cr^{3+} replaces W^{4+} in WSe_2, it forms new energy states, effectively modifying the band structure. Indeed, previous studies on Cr in WSe_2 have reported the emergence of Cr^{3+} peaks in XPS along with an electron surplus, indicating that electron accumulation rather than hole generation occurs.[40] These results further support our interpretation that $W_{1-x}Cr_xSe_2$ can withdraw electrons from WSe_2 at the interface. Consequently, the $W_{1-x}Cr_xSe_2$ interface may act as a negative interface dipole between WSe_2 and Cr, facilitating the reduction of the SBH.

It is essential to understand how the band structure is modified at the WSe_2/Cr contacts. The characteristics of a metal−semiconductor junction are determined by the Schottky−Mott rule.[44] The ideal SBH for holes is defined as

$$\Phi_{SBH,h} = E_g + \chi_s - \Phi_M$$

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where $\Phi_{SBH,h}$ represents the SBH for holes and E_g, χ_s and Φ_M refer to the bandgap of the semiconductor, electron affinity, and work function of the metal, respectively. For achieving a p-type ohmic contact, the condition $\Phi_M > E_g + \chi_s$ must be satisfied. Since $E_g + \chi_s \approx 5.2$ eV for WSe_2, a high work-function metal (>5.2 eV, such as Pd or Pt) is required for p-type operation (Figure 3(a)). But even with high work-function

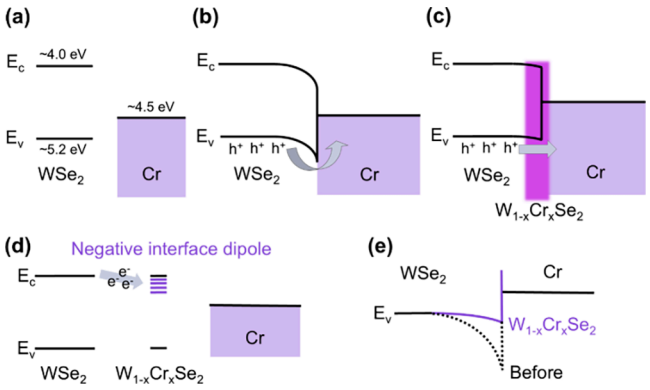

Figure 3. Band diagrams of the WSe_2/Cr contact before and after alloying. (a) Energy band structures of pristine WSe_2, including conduction band minimum, valence band maximum, and the work function of Cr. (b) Band alignment at the WSe_2/Cr contact before alloying, showing a significant Schottky barrier. (c) Modified band alignment after alloying, indicating reduced SBH. (d) Schematic illustration of the band structure and charge transport mechanism between WSe_2 and $W_{1-x}Cr_xSe_2$. (e) Schematic band diagram showing the reduction of SBH at the WSe_2/Cr interface induced by the negative interface dipole of the $W_{1-x}Cr_xSe_2$.

materials, p-type operation is not guaranteed due to FLP.[13,14] The work function of Cr is approximately 4.5 eV, which is insufficient to realize a p-type ohmic contact with WSe_2. Therefore, as shown in Figure 3(b), the WSe_2/Cr contact exhibits a high SBH. However, the $W_{1-x}Cr_xSe_2$ can be readily formed at the Cr−WSe_2 interface. The reported band structure and p-type properties of $W_{1-x}Cr_xSe_2$ are expected to enhance hole transport.[31,32,45,46]

Cr introduces energy states below the conduction band minimum of WSe_2 and narrows the bandgap, thereby allowing electrons from WSe_2 to be captured, as shown in Figure 3(d). The accumulated electrons in these energy states act as a negative interface dipole, effectively lowering the SBH between Cr and WSe_2. This phenomenon can be quantitatively explained using the affinity rule. The affinity rule between WSe_2 and $W_{1-x}Cr_xSe_2$ is defined as follows:[47]

$$\Delta E_c = \chi_{W_{1-x}Cr_xSe_2} - \chi_{WSe_2}$$

$$\Delta E_v = (\chi_{WSe_2} + E_{g,WSe_2}) - (\chi_{W_{1-x}Cr_xSe_2} + E_{g,W_{1-x}Cr_xSe_2})$$

where ΔE_c represent the potential differences at the conduction band and ΔE_v represents that at the valence band. χ and E_g represent the electron affinity and the bandgap, respectively. For $W_{1-x}Cr_xSe_2$, the increase in χ is offset by a corresponding decrease in E_g. This results in an almost constant $\chi + E_g$ value between WSe_2 and $W_{1-x}Cr_xSe_2$, and consequently $\Delta E_v \approx 0$. Meanwhile, the decrease in ΔE_v allows electrons in the conduction band of WSe_2 to transfer into the new energy states of $W_{1-x}Cr_xSe_2$, producing an effect equivalent to a negative interface dipole. This mechanism involves band structure modification, which is expected to reduce the SBH between the Cr and WSe_2 interface, Figure 3(e).

The exact band structure and work function of $W_{1-x}Cr_xSe_2$ formed by alloying are unknown. Therefore, it is necessary to extract the SBH quantitatively. The SBH of the $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs was extracted and compared with that of pristine Cr contact WSe_2 FETs. Temperature-dependent transfer characteristics of pristine Cr contact and $W_{1-x}Cr_xSe_2$ contact WSe_2 FETs were measured from 110 to 290 K, as shown in Figures 4(a) and 4(c). The SBH was

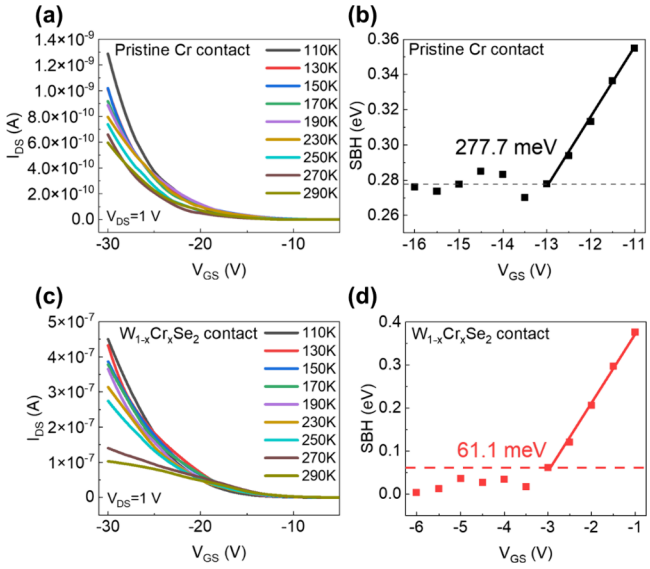

Figure 4. Temperature-dependent transfer characteristics (110−290 K) and corresponding SBH. (a), (c) Transfer characteristics of pristine Cr contact and $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs, respectively. (b), (d) SBH extracted from (a) and (c).

extracted by measuring the activation energy in the thermionic emission regime using the two-dimensional (2D) thermionic emission equation.[48−50] The 2D thermionic emission equation is given by

$$I_{DS} = AA^*T^2 \exp\left[-\frac{q\Phi_{B0}}{k_BT}\right] \times \left[1 - \exp\left(-\frac{qV}{k_BT}\right)\right]$$

where A is the contact area, A^* is the Richardson constant, T is the temperature, q is the electronic charge, k_B is the Boltzmann constant, and Φ_{B0} is the SBH. Under the condition $qV \gg k_BT$, the equation simplifies to

$$I_{DS} = AA^*T^2 \exp[-q\Phi_{B0}/k_BT]$$

For 2D semiconductor devices, the common form of the Arrhenius plot is $\ln(I_{DS}/T^{3/2})$ versus $1000/T$. From the transfer curve in Figures 4(a) and 4(c), the Arrhenius plots were extracted, and their slopes (Figure S3) correspond to the activation energy E_A.

$$E_A = q\Phi_{B0} - (E_C^\infty - E_C^0)$$

Here, E_A represents the total activation energy required for carriers to be injected from the contact into the channel. Under flat-band conditions $E_C^\infty - E_C^0 = 0$, and when $V_{GS} < V_{FB}$, E_A varies linearly with gate bias. Therefore, in Figures 4(b) and 4(d), the point where the linear region deviates are considered the flat-band voltage, which allows extraction of the SBH

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(Φ_{B0}). Using this method, the SBH of the pristine Cr contact and $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FET were evaluated to be 277.7 and 61.1 meV, respectively. These results demonstrate that the $W_{1-x}Cr_xSe_2$ interface formed by alloying between Cr and WSe_2 effectively reduces the SBH. This suggests that thermal alloying generates a negative interface dipole and can induce a favorable band alignment for p-type operation, independent of the constraints imposed by FLP. The SBH was reduced by approximately 4.5 times through the formation of a $W_{1-x}Cr_xSe_2$ interface. This alloy engineering enables a favorable band structure for hole injections, alleviating the limitations typically imposed by FLP.

When the SBH is reduced by $W_{1-x}Cr_xSe_2$ interface, hole carrier transport from the source/drain toward the channel is facilitated. This implies a decrease in the contact resistance of the WSe_2 FETs. Accordingly, contact resistance was extracted and analyzed to evaluate how effectively the $W_{1-x}Cr_xSe_2$ interface reduces it. Due to fabrication challenges in constructing a Transfer Length Method (TLM) test structure for WSe_2 flakes transferred by the Scotch tape method, the contact resistance is instead evaluated using the Y-Function Method (Y-FM). When applying the Y-FM to back gate TMD devices, device-to-device variation must be considered, as variability can occur even under identical fabrication conditions, potentially causing inaccuracies. Because Y-FM is highly sensitive to channel length, it often overestimates contact resistance, with the most reliable value obtained from the shortest channel devices. However, fabrication limits confine the channel length to the μm scale, hindering ideal contact resistance extraction. Furthermore, for global back gate devices, the gate bias can influence the Schottky barrier at the source/drain.[51,52]

In this study, variation in channel length and contact area across the exfoliated WSe_2 flakes introduces additional uncertainty in contact resistance evaluation due to these back-gate devices. Therefore, it is more reasonable to examine the statistical trend across a set of devices. Contact resistance for 8 devices was evaluated using the Y-FM, as shown in Figure S5 and Table S3. The extracted Y-function resistance before and after alloying is summarized in Figure 5(b) (quantitative values are provided in Table S3). Prior to alloying, the contact resistance is evaluated to be on the order of tens of MΩ, which is comparable to previously reported values for Cr contacts.[53]

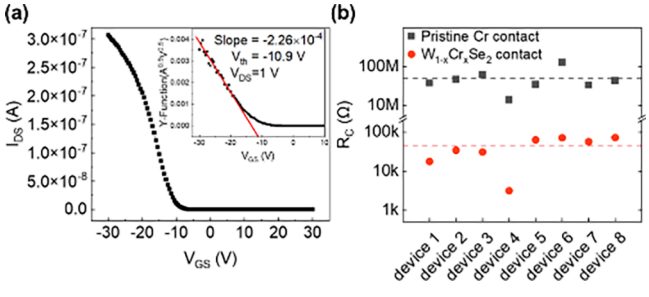

Figure 5. Extraction of contact resistance through the Y-Function Method. (a) Transfer curve of $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FET (linear scale) and slope with threshold voltage (V_{th}) extracted from the Y-Function. (b) Comparison of contact resistance before and after alloying, extracted from 8 devices. The average contact resistance was measured to be 50.0 MΩ for pristine Cr contact (black) and 43.9 kΩ for $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs (red).

After alloying to form a $W_{1-x}Cr_xSe_2$ alloy interface contact, the contact resistance is significantly reduced to the range of several to tens of kΩ (with a minimum value of 3.14 kΩ), representing an average reduction of approximately 3 orders of magnitude.

The variation in contact resistance is thought to arise from slight differences in the thickness or morphology of the WSe_2 flakes. Despite the inherent variation and limitations in back-gate WSe_2 FETs, these results clearly demonstrate that the $W_{1-x}Cr_xSe_2$ alloy interface effectively reduces contact resistance and facilitates hole carrier transport as a result of low SBH.

Figures 6(a) and 6(b) present the transfer characteristics of the $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FETs, compared with pristine Cr contact WSe_2 FETs. The measurements were performed at room temperature with V_{DS} = 1 V. Due to their relatively low work function (~4.5 eV), Cr contacts lead to ambipolar behavior in WSe_2 FETs and are further affected by FLP. The threshold voltage shift likely results from the removal of interfacial residues and slight refinement of the WSe_2/SiO_2 interface properties upon thermal annealing.[54−56] The observed improvements in transfer characteristics following alloying indicate that the $W_{1-x}Cr_xSe_2$ interface enables robust p-type operation, regardless of FLP. Enhancement occurred only for hole-current, with minimal or no change in the electron current. This trend was consistently observed across 20 devices, demonstrating both the reproducibility and reliability of p-type behavior (Figures S4 and S5). On average, the on-current (I_{ON}) increased by a factor of approximately 600, while the off-current (I_{OFF}) remained nearly unchanged (Figure 6(c)). The devices exhibited a maximum on/off current ratio of ~5×10^8, with an average value of 2.19×10^8, indicating high performance.

Ti contacts (work function ~ 4.5 eV), comparable to Cr, were also employed for comparative analysis. (Figure S6) In the case of Ti, hole current enhancement was observed beginning at 300 °C, coupled with an increase in electron current as well, resulting in continued ambipolar behavior. The observed enhancements in on-current are attributed to improved interfacial coupling rather than changes in the band structure.[28] Furthermore, after annealing at 400 °C, the I_{OFF} increased significantly, degrading the on/off ratio. These comparisons support the conclusion that the improved hole transport in Cr−WSe_2 devices arises not from a simple interfacial interaction due to thermal annealing, but rather from the formation of $W_{1-x}Cr_xSe_2$, which provides a band structure favorable for hole conduction.

Figures 6(d) and 6(e) display the output characteristics of the WSe_2 FETs measured with V_{GS} ranging from −30 to −10 V in 2 V steps. The pristine Cr contact WSe_2 FET exhibits nonlinear output characteristics due to a large SBH, whereas the $W_{1-x}Cr_xSe_2$ alloy interface contact WSe_2 FET shows quasi-ohmic behavior, consistent with a low SBH. Furthermore, as shown in Figure 6(f), the two-terminal characteristics measured under floating gate bias become significantly more linear after alloying, with the current level enhanced by nearly 3 orders of magnitude. These electrical properties strongly support the conclusion that the $W_{1-x}Cr_xSe_2$ formed in the source/drain regions effectively improves the contact interface for hole carrier injection through the reduction of the SBH.

SBH achieved in this work compared with those reported for representative p-type WSe_2 contact engineering approaches, including vdW contact and doping techniques. Recent vdW

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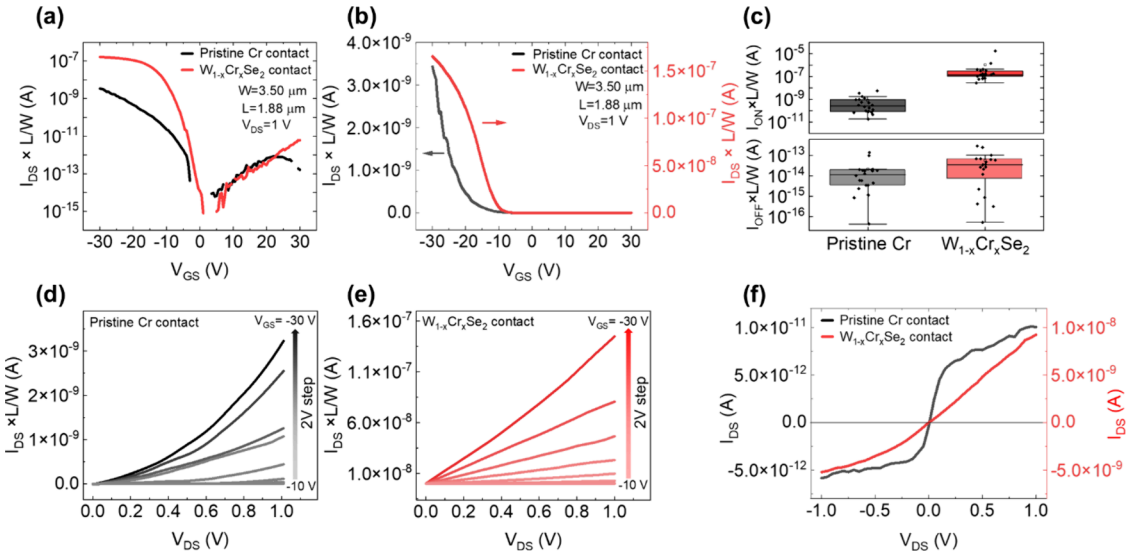

Figure 6. Electrical characteristics of WSe_2 FETs Cr contact and $W_{1-x}Cr_xSe_2$ alloy interface contact. (a), (b) Transfer characteristics plotted on logarithmic and linear scales, respectively, with the pristine Cr contact device (black line) and the $W_{1-x}Cr_xSe_2$ contact device (red line). (c) Statistical comparison of on-current (top graph) and off-current (bottom graph) for 20 devices, with black boxes representing the pristine Cr contact device and red boxes representing the $W_{1-x}Cr_xSe_2$ contact devices. (d), (e) Output characteristics of pristine Cr contact and $W_{1-x}Cr_xSe_2$ contact WSe_2 FETs, respectively. (f) Two-terminal characteristics comparing pristine Cr contact (black line) and $W_{1-x}Cr_xSe_2$ contact (red line).

contact strategies have demonstrated excellent performance by reducing the SBH to several tens of meV. Representative examples include P^+-MoS_2/WSe_2 (~41 meV), laser doping with $TaSe_2$ vdW contact (~65 meV), and TTT molecular doping with TiS_2 contacts (~43.4 meV).[22,25,57] However, these approaches typically involve complex transfer or synthesis processes, which limit their scalability. Additionally, WO_x doping assisted contacts can enhance p-type transport, but they typically exhibit higher SBH values (~260 meV).[20] A detailed comparison with recent studies is summarized in Table S2. The contact strategy proposed in this study achieves a comparable SBH of 61.1 meV through a CMOS-compatible, single-step thermal process, without requiring additional transfer or chemical doping procedures. This approach offers a reliable and scalable pathway for integrating p-type contacts into high-performance WSe_2 FETs.

CONCLUSIONS

This study demonstrated that $W_{1-x}Cr_xSe_2$ alloy interface contacts formed by RTP significantly enhance the performance of p-type WSe_2 FETs. The alloy interface effectively reduces the SBH to as low as 61.1 meV, leading to greatly improved hole injection and transport. Consequently, the contact resistance can be reduced by approximately 1000 times. Electrical characterization showed that the on-state current increased by up to 600 times while maintaining a low off-state current, achieving high on/off ratio of approximately 10^8. These results confirm that the $W_{1-x}Cr_xSe_2$ alloy interface offers a simple, scalable, and cost-effective approach to enhance p-type contacts in WSe_2 devices, presenting strong potential for practical applications in future CMOS technologies.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.5c18346.

Fabrication process of WSe_2 FETs, Raman spectra comparison before/after alloy and Cr related modes, Arrhenius plots and comparison with previous vdW contact studies, transfer characteristics of WSe_2 FETs after RTP at various temperatures (200−600 °C), transfer curves of pristine vs Cr alloy WSe_2 FETs and Y-Function Method extraction, and transfer curve of WSe_2 FETs with Ti contacts after RTP at various temperatures (300−600 °C) (PDF)

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Author Contributions

Y.-J.S. and H.-J.K. conceived the concept. Y.-J.S. and J.K. fabricated and characterized the device. Y.-J.S. and J.L. conducted the experiments. Y.-J.S. wrote the paper. All authors discussed the results and commented on the manuscript. H.-

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J.K. was responsible for managing all aspects of this project. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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