Ph.D Thesis
박사 학위논문

Fabrication and Characterization of Amorphous InGaZnO Thin Film Transistor for Flexible Devices

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DGIST

2018

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A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Information and Communication Engineering. The study was conducted in accordance with Code of Research Ethics[1]

11. 22. 2017

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[1] Declaration of Ethical Conduct in Research: I, as a graduate student of DGIST, hereby declare that I have not committed any acts that may damage the credibility of my research. These include, but are not limited to: falsification, thesis written by someone else, distortion of research findings or plagiarism. I affirm that my thesis contains honest conclusions based on my own careful research under the guidance of my thesis advisor.

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이 광 준. Gwnagjun Lee. Fabrication and Characterization of Amorphous InGaZnO Thin Film Transistor for Flexible Devices. Department of Information and Communication Engineering. 2018. 100p. Advisors Prof. Jae-eun Jang, Co-Advisors Prof. Hongsoo Choi.

ABSTRACT

The current interest in transparent amorphous oxide semiconductor (AOS) thin film transistors was performed in operation of amorphous indium gallium-zinc oxide, a-IGZO, TFTs on flexible, room temperature and polymer substrate. AOS area has rapidly developed, with a-IGZO TFT addressed active matrix displays. AOS are a new area of materials with electrical and optical characteristics uniquely suited to transparent, flexible and large area electronics. The a-IGZO TFTs have considerable attracted interest due to a room temperature processing, a visible transparency and a large area uniformity. These are ideal properties for using them as active layers in TFTs which form the backbone of active matrix display and large area electronic applications. Nevertheless, for these devices to be commercially viable for flexible electronics, new device design concepts with an electrically analysis of device operation and reliability should be considered. In this dissertation, a-IGZO TFTs on various substrates were studied in the respect of material characteristics, the design of device and its electrical performances.

One of the key features of a-IGZO TFTs have a much higher field-effect mobility

(μ_{FE} = >10 $cm^2/V \cdot s$) compared to a-Si:H TFTs, a low threshold voltage exhibiting in enhancement mode operation, excellent switching properties, and a small parasitic series resistance employing IZO as source/drain electrode without the additional contact doping process. Process optimization of a-IGZO TFT was performed in scaling channel length, temperature-dependence and oxygen dispersion on active surface.

A bendable a-IGZO TFTs and inverter circuits was demonstrated on a thin glass substrate. From the bending tests on the TFTs, V_{TH} was negatively shifted as an increase of the bending strain for the symmetric gate overlap sample, while the TFTs showed relatively stable operation against mechanical strain for the asymmetric gate overlap sample. Owing to the high temperature thermal annealing process, the a-IGZO TFTs showed very good bias stress stability under prolonged positive and negative stress test. Therefore, transparent, flexible, and stable TFTs can be realized using the a-IGZO TFTs on the thin glass substrate which can open a new topic for flexible display applications.

Finally, we demonstrated high performance and flexible a-IGZO TFTs with hole-array on polyimide substrate and investigated the variation in the electrical characteristics as a function of hole area and radius. The a-IGZO TFTs with hole-array device performance shows good electrical characteristics and the mechanical strain reduced remarkably in hole-array structure as compared with the TFT without hole-array. Electrical stability measurements of the flexible devices with hole-array structure under tensile and compres-

sive mechanical strain showed no appreciable change in the I-V characteristics during bending. The electrical characteristics under mechanical bending suggest that carrier transport was unaffected during mechanical strain. Testing under dc gate bias conditions, the electrical stability of the TFTs showed a positive V_{TH} shift of 3.8 V after 3600 s without any change in subthreshold-swing (S.S.). The a-IGZO TFTs with hole array structure exhibits high on/off ratio of $>10^6$ and field effect mobility of >6 $cm^2/V \cdot s$ even after high bending radius. The bending radius was set to 100 mm by considering minimum bending radius (tensile strain of 0.22 % perpendicular to the channel current flow). The a-IGZO TFTs with hole-array remarkably reduced more electrical failure than TFT without hole-array samples since disconnected micro-cracks induced the release of mechanical strain. Thus, proposed hole-array structure of a-IGZO TFTs can give an important merit to use flexible devices.

Keywords: Oxide TFT, Flexible Device, Flexible Electrodes, Flexible Circuits, Flexible sensors

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Ⅰ. INTRODUCTION

1.1 Background and Motivation

The flat panel display industry has been built around TFTs with rigid glass substrate, but there are well-identified applications requiring flexible substrate. Recently, transparent flexible electronics have received great attention in active-matrix organic light-emitting diode (AMOLED) displays for large-area electronics applications ranging from displays and smart window systems to flexible sensor arrays. The main challenges in this area is fabricating high-performance and transparent flexible thin film transistors (TFTs). The different active materials such as amorphous silicon (a-Si), organic semiconductors and low temperature polysilicon (LTPS) can be used as active layers of TFTs. A amorphous Si has the advantages of both uniformity including a large-area and maturity in fabrication process. Due to the insufficient field-effect mobility of its material system, it is not possible to apply this class of TFTs to fabricating large area and high performance LCD displays. The electrical instability of a-Si is another drawback that restricts its application in the display industry. Furthermore, cause of the poor electrical stability and field-effect mobility of organic materials, there is less possibility of this class of TFTs being used as an alternative for a-Si and LTPS in the immediate future. Several research groups have announced that grain boundary is the main factor in the deterioration of short-range uniformity.

Table 1-1 Comparison of Different TFT Technolody

TFT properties	Oxide semiconductor	Amorphous Si	Low-T poly-Si	Organic semiconductor
Carrier mobility [cm^2/Vs]	Good	Bad	Best	Not bad
Long term TFT reliability	High	Low	High	Low in air
Transparency	Good	Not bad	Not bad	Bad
Yield	High	High	Medium	High
Biocompatibility	Good	Good	Good	Not bad
Process temperature [°C]	RT to 350	~250	<500	RT

Hence, high-field-effect mobility amorphous semiconductors will be an ideal candidate in developing large-area high-performance electronics. However, many researchers used to well known that the field effect mobility of metal oxide semiconductors significantly deteriorates after switching from crystalline structure to the amorphous phase.

This degradation effec had been attributed to the strong scattering from disordered structures, and deterioration of about 1500 $cm^2/V{\cdot}s$ in crystalline silicon (c-Si) structures to less than 2 $cm^2/V{\cdot}s$ in amorphous structures had been considered the essential proof.

However, Hosono et al. achieved this understanding by demonstrating high carrier mobility amorphous metal oxides composed of heavy metal cations. They later completed amorphous metal oxides by taking advantage of the spherical shape of the s-orbitals in the conduction band, are insensitive to exhibit large band-dispersion and overlaps even in amor-

phous structures. This large band dispersion results in high mobility in the amorphous structure of this material system. Valence band maximum (VBM) and conduction band minimum (CBM) are made up from the anti-bonding and bonding states of hybridized orbitals, respectively.

Large spatial directionality results in the formation of the strained chemical bonds and large amount of traps and scattering centers in amorphous structures. It explains why much lower field-effect mobility is observed in conventional amorphous structures such like hydrogenated amorphous silicon than in crystalline silicon.

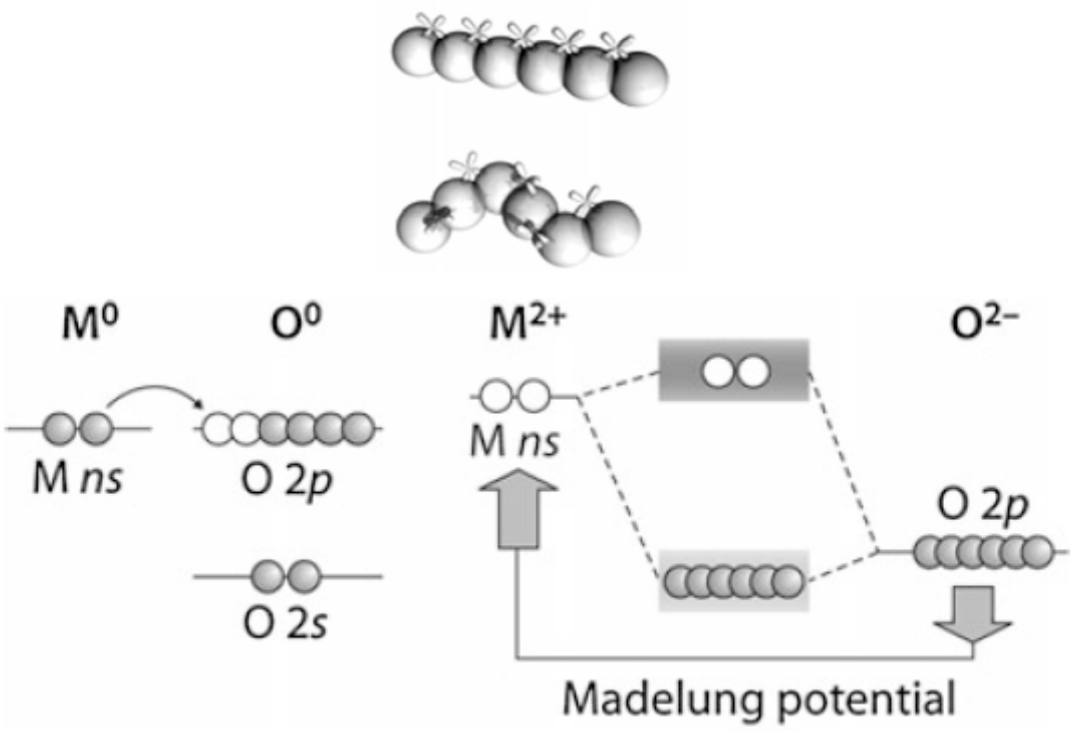

Figure 1-1 Schematic diagram of charge transfer and band gap formation process in ionic oxide semiconductor.

The unique electronic properties of oxides semiconductor have attracted interest in several transition metal oxides such like ZnO, In_2O_3 and SnO_2, all have large spherical shape s-orbitals in their conduction bands. In nature, these oxides are polycrystalline and cannot be considered as TFT channel layer material due to their poor electrical properties. Nevertheless, taking advantage of different crystalline structures and different coordination numbers to the oxygen, each component of the above mentioned oxides can result in the formation of amorphous structures with a large spherical shape s-orbital in their conduction band. The ZnO and In_2O_3, by having wurtzite and bixbyite structures, respectively, it demonstrating different coordination numbers to oxygen as ZnO_4 and InO_6, can result in the formation of a high field-effect mobility amorphous InZnO (IZO) structure. The structure can be considered as both semiconductor channel layers and transparent electrodes, depending on its chemical composition. Amorphous IZO shows high field-effect mobility of above 15 $cm^2/V \cdot s$ and superior uniformity in electrical properties, the presence of high carrier concentration in this material system even at low In content results in a large off-current (I_{off}) and small Ion/off ratio, which hinders its application as a TFT channel layer. This problems has been overcome by the incorporation of Ga into the IZO structure and results in the formation of an amorphous IGZO channel layer. Nomura et al. showed that Ga ions tightly bind oxygen ions, thereby supressing the formation of oxygen deficiency, which are considered to be shallow donors in the IGZO channel layer material. IGZO TFTs have superior field-effect mobility and electrical stability than a-Si.

The good electrical stability is cause of the presence of lower density of states in their sub-bandgap energy. Also amorphous metal oxides have much better electrical uniformity than LTPS. As a consequence of those benefits, the semiconductor oxides have been suggested as one of the most promising candidates for large-area electronic.

The metal oxides demonstrate high optical transparency due to their large band-gap energy, which makes them one of the key components in the field of transparent electronics. Their amorphous structure is better suited for large-area processes cause of absence of the grain boundaries. All of these unique advantages have resulted in such rapid development of IGZO TFT technology, Sharp demonstrated the first IGZO TFT-based LCD display almost eight years Hosono et al. introduced high-performance working on amorphous IGZO active layer. But, many scientific reports have continued to be published since demonstration of the first LCD panels incorporating IGZO TFTs that continue to address remaining problematic areas. There was an upward trend in the number of such publications. Both the upward trend and the volume of these publications suggest that although many developments have occurred in the field of TFTs, some issues remain in developing a conventional and low-temperature process for fabrication of IGZO based-large-area flexible transparent electronics.

Recently, several research groups have reported the feasibility of fabricating high-performance flexible IGZO TFTs. Recent papers report the research on flexibles IGZO TFTs on different flexible substrates such as flexible glasses and polymeric substrates. It

also compares these studies in terms of the conventional dielectric layers used, optical transparency, source/drain patterning techniques, and their electrical stability.

There is a lack of understanding with regards to the electrical stability of these devices where long-term aging tests would provide insight to the operational lifetimes for flexible a-IGZO TFTs. A closer look at the findings of these reports concludes that their fabrication processes involve two main approaches such as mechanical structure techniques and applying high-temperature processes that limit fabrication to high melting-point substrates such as polyimide, and flexible glass substrates. Greater understanding of the electrical instability of the flexible TFTs is also needed. Thus, it is clear that if large-area flexible transparent electronics based on IGZO TFT with hole structures are to be developed, it will be critical to overcome the engineering and scientific challenges to enable fabrication processes for high-performance flexible transparent IGZO TFTs enable the current state-of-the-art large-area electronic systems.

1.2 Flexible Electronics

Thin-film electronics in its myriad forms has underpinned much of the technological innovation in the fields of displays, sensors, and energy conversion over the past four decades. This technology also forms the basis of flexible electronics. Additionally, flex circuits can be screen printed silver circuits on polyester. Flexible electronic assemblies may be manu-

factured using identical components used for rigid printed circuit boards, allowing the board to conform to a desired shape, or to flex during its use. Flexible electronics have an emerging technology consisting of robust, light weight, conformal, and bendable electronic systems. Due to the unique properties, flexible electronics enables applications in advanced large-area electronics for displays, sensors, medical devices, and solar cells that can bend and fold. The first step in the fabrication of flexible transparent electronic devices is choosing an appropriate flexible substrate. The ideal flexible substrate needs to be rollable, and transparent.

It needs to be resistant against chemical attack, have low permeability to water and oxygen, and to be dimensionally stable under thermal processing steps. Flexible substrates can be divided into three main categories such like flexible glasses, polymeric substrates and metal foil. Metal foils have strong resistance to water vapor and oxygen diffusion. In addition, metal foils have a low coefficient of thermal expansion (CTE). However, due to their high conductivity and the relatively rough surface of metal foils, it need to be coated by an insulating spin on glass planarization layer before being applied as flexible substrates in device fabrication processes. Flexible substrate is thin glass plates. Flexible glass substrates provide perfect barrier layer and superior optical transparency properties against oxygen atoms. However, this class of flexible substrates is highly sensitive to breaking and cracking, preventing their application in large-area flexible electronics. The third category of flexible substrates is the polymeric substrates, among which polyethylene napthalate (PEN), polyethersulfone (PES), polyethylene terephthalate (PET), polycarbonate (PC), and Polyimide

(PI) film have been extensively studied as flexible substrates.

Among the above-mentioned candidates, PI and PEN substrates prefer due to it has high transparency, compatibility with microfabrication processes, and high Young's module. In addition, its thermal and dimensional properties are better than PET substrates.

However, due to the low thermal resistance and high thermal expansion of polymeric substrates, in PI substrate, the maximum process temperature needs to be lower than 400°C.

Low-temperature processed high-performance TFT is one of the most challenging areas in developing large-area flexible electronics. Several reports have demonstrated fabrication of TFTs on flexible substrates based on different channel layer materials such as amorphous silicon, low-temperature polycrystalline silicon, organic semiconductors and metal semiconducting oxides. However, many of these materials do not possess these requirements for high performance large-area devices. The TFTs have demonstrated acceptable electrical characteristics with good uniformity, high field-effect mobility and low threshold voltages even low temperatures. Among them, oxide TFTs are one of the most promising candidates for the development of large-area transparent flexible electronics due to the both the function of transparency and the good electrical properties even though at low temperature processing.

1.3 Organization of Dissertations

This dissertation focuses on design, fabrication and characterization of a-IGZO TFTs on mostly flexible thin substrates. A brief review of present status of amorphous oxide based materials is presented first in chapter 1 and 2. In chapter 3, the scaling behaviour of amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) were analysed with amorphous indium zinc oxide (a-IZO) transparent source/drain (S/D) electrodes. Due to the sputtering damage of the back-channel region during the a-IZO deposition process, the output characteristics show early saturation behaviour and the field-effect mobility in the saturation region is severely decreased in comparison with that in the linear region, especially when the channel length is decreased. Based on the transmission line method, we found that a long gate overlap distance is required due to the long current transfer length. Therefore, optimizing the parasitic resistance is required for the scaling down of a-IGZO TFTs with transparent a-IZO S/D electrodes. In chapter 3, electrical properties of transparent amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) with amorphous indium zinc oxide (a-IZO) transparent electrodes on a flexible thin glass substrate was investigated. The TFTs show a high field-effect mobility, a good subthreshold slope and a high on/off ratio owing to the high temperature thermal annealing process which cannot be applied to typical transparent polymer-based flexible substrates. Bias stress instability tests applying tensile stress concurrently with the bending radius of up to 40 mm indicated that

mechanically and electrically stable a-IGZO TFTs can be fabricated on the transparent thin glass substrate. Device (a-IGZO TFT based) fabrication on flexible structure is presented next with comprehensive electrical analyses to characterize a-IGZO TFTs on flexible substrate. The electromechanical stability of a-IGZO TFTs with hole structure on flexible substrate is introduced in chapter 5. Finally, the concluding chapter summarizes this Ph.D. thesis to the field of flexible transparent electronics and points out suggestions for future work.

II. PROCESS OPTIMIZATION AND ELECTRICAL CHARACTERIZATION OF a-InGaZnO THIN FILM TRANSISTOR

2.1. Introduction

As we have noted in the introductory chapter, thin film transistors (TFTs) have significant technological importance in displays and other large-area electronic applications. Nevertheless, the range of applications possible from these TFTs have been somewhat limited by their overall poor performance on low cost substrates compared to conventional silicon MOSFETs. This poor performance can be characterized using several measures, including field-effect mobility, subthreshold slope, device hysteresis, and bias stress stability. More importantly, these parameters have implications towards the implementation of TFTs in real applications. Additionally, at a more fundamental level, all of these parameters reveal important electrical characteristics of the semiconductor thin films, the interface between semiconductor and the dielectric layers and robustness of the device processing; therefore, by fabricating TFTs one provide useful measure of the electrical properties of new materials, which in turn can aid the development of real application demonstrations. Untill now, large area flexible systems are enabled by a-Si:H or organics which suffer from low mobilities that limit their use in driver electronics that require higher current drive. Amorphous oxide TFTs are an attractive alternative to traditional thin film silicon (Si) based devices since they offer several key advantages such as high mobilities, transparency in the visible spectrum and low processing temperature. As flexible substrate materials, thin glass and flexible plastics have been used with demon-

stration of high performance devices and systems. We chose to fabricate such TFTs on thin glass and polyimide, since they offer high mechanical strength, flexibility, light weight as well as greater dimensional stability which afford small geometry features of the devices and circuits. In this chapter we will discuss the process optimization of amorphous oxide TFTs fabrication on Si and glass substrate. Given that the main focus of this study is on the optimization of oxide semiconductor for application in TFTs and other large area electronic circuits, electrical characterization of standalone devices are discussed in details in the second half of this chapter.

2.2 Scaling channel length effect of a-IGZO TFTs with a-IZO electrodes

Recently, high performance amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) have been intensively investigated with regard to their applications to flexible and rollable display devices as well as conventional LCD display devices. In addition, the a-IGZO TFTs are also considered to be a candidate for next-generation transparent or see-through display devices. Thus far, various oxide-based alloys, such as amorphous indium zinc oxide (a-IZO) and indium tin oxide (ITO), have been considered as transparent electrodes. However, there are few reports about the electrical behaviour of a-IGZO TFTs having a short-channel length with transparent source/drain (S/D) electrodes. In fact, most of the previous works that analysed the electrical properties of a-IGZO TFT with transparent S/D electrodes were performed for TFTs with a long-channel length. In such a case, the current

driving capability is decreased, which eliminates the advantage of the high field-effect mobility of the a-IGZO TFT. Therefore, for practical applications of a-IGZO TFTs with transparent S/D electrodes, the scaling down of the channel length and an accompanying analysis of the electrical characteristics are required. In particular, an extraction of key parameters such as the field-effect mobility and the parasitic resistance should be carried out for further optimization of the performance of a-IGZO TFTs.

In this dissertation, we studied the scaling down behaviour of a-IGZO TFTs with transparent a-IZO S/D electrodes. The field-effect mobility, current transfer length and the parasitic resistance were analysed as functions of the channel length and the gate-to-source voltage (V_{GS}). The transmission line method (TLM) was used for a systematic analysis of the electrical characteristics.

Figure 2-1 shows the fabrication steps of a-IGZO TFT employing an inverted staggered bottom gate structure. A heavily doped n-type Si wafer was used as a substrate and a gate electrode. A 200 nm thick SiOx gate insulator was formed by a wet oxidation process. After that, the active layer of the a-IGZO (InGaZnO4 target) semiconductor (80 nm) was sputtered by a radio-frequency magnetron sputtering system at a gas mixing ratio of Ar/O2 = 50/5 (sccm/sccm), and at an input power and pressure of 400W and 5mTorr, respectively. It should be noted that in order to eliminate the gate overlap variation effects on the parasitic resistance, the active islands were patterned to be under the S/D electrodes by photolithography and the wet-etching process. Then, the 100 nm thick indium zinc oxide (IZO, In_2O_3 : ZnO = 9 : 1 mol% target) layer was sputtered by dc magnetron sputtering at a gas mixing ratio of Ar/O_2 =

120/5 (sccm/sccm), and an input voltage and pressure of 400V and 5mTorr, respectively.

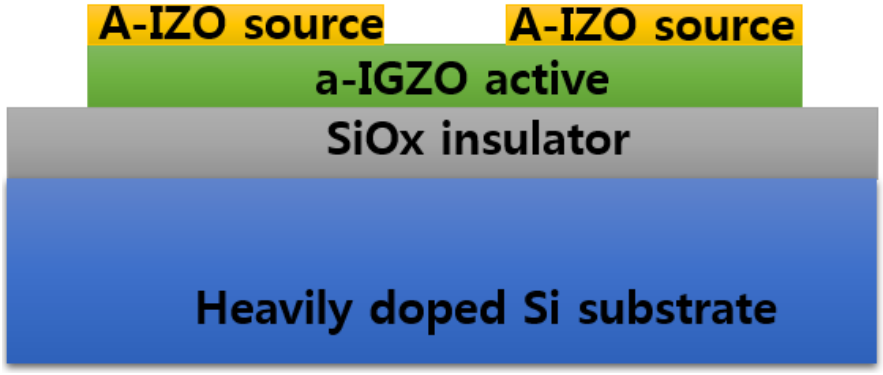

Figure 2-1. Fabricated a-IGZO TFT with heavily doped Si substrate.

The electrical characteristics of a-IZO layer were analysed by the van der Pauw method. The carrier density, Hall mobility and resistivity of the a-IZO layer were about 3.5×1020 cm^{-3}, 33cm^2 V^{-1} s^{-1} and 5.3 × 10−4 Ω cm, respectively. The S/D electrodes were formed by a lift-off process. Finally, the TFTs were annealed at 300 ◦C for 1 h in ambient oxygen. The minimum target channel length was 2μm, while the minimum value of channel length as measured by a microscope was about 3μm due to process variations during the lift-off process. A Keithley 4200 semiconductor analyser was used to measure the I–V characteristics in ambient air.

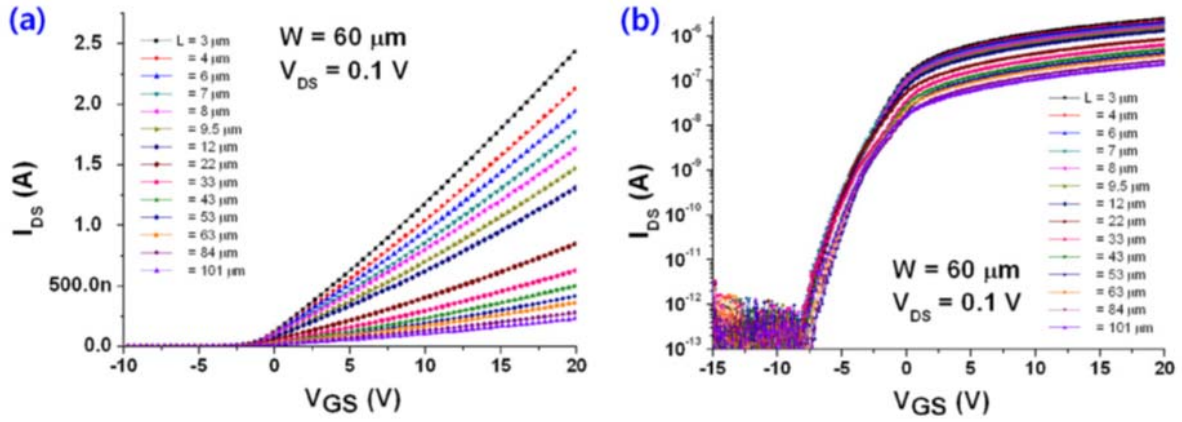

Figure 2-2. Transfer characteristics of a-IGZO TFTs with L from 3 to 101μm in (a) linear scale and (b) log scale.

Figures 2-2(a) and (b) show the transfer characteristics of a-IGZO TFTs with channel lengths (L) ranging from 3 to 101μm in linear and log scale, respectively. The on/off ratio was larger than 10^7 A/A and the subthreshold slope was about 0.6 V/decade. These parameters were independent of channel length variations. The transfer curves show good linearity for the short- and long-channel length TFTs without any rollover behaviour.

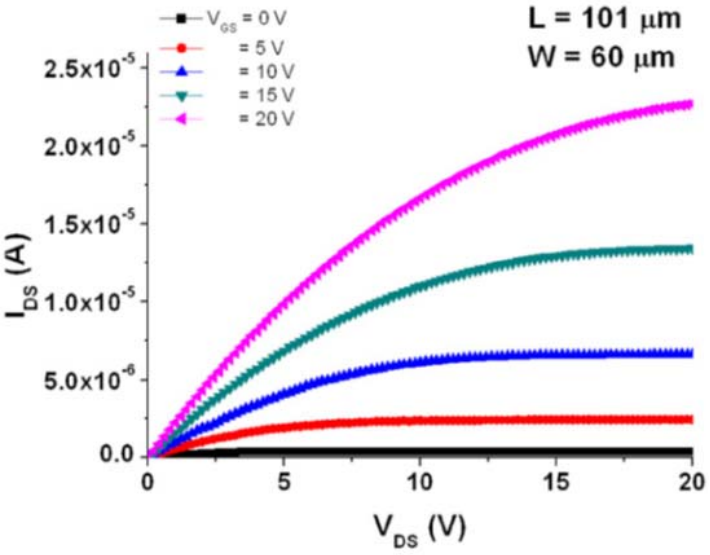

Figure 2-3. Output characteristics of a-IGZO TFT with L = 101μm.

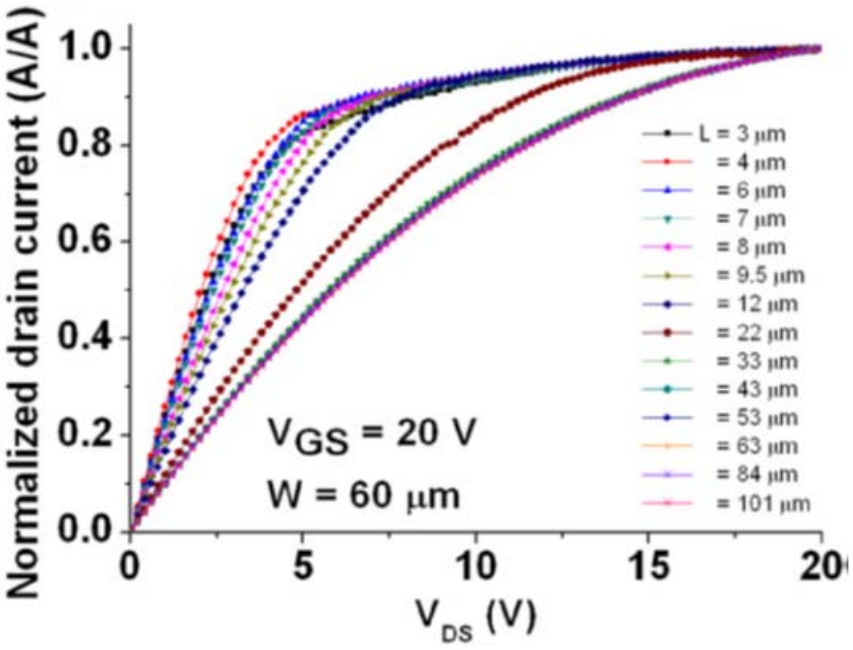

Figure 2-4. Normalized output characteristics of a-IGZO TFT with L from 3 to 101μm.

Figure 2-3 shows the output characteristics of a-IGZO TFTs with L = 101μm. The result shows typical output characteristics with good saturation behaviour. However, the output characteristics of the TFTs with short-channel length were quite different from those with long-channel lengths. Figure 2-4 shows the normalized output characteristics of a-IGZO TFTs (normalized according to the maximum drain current for different V_{GS}) with different channel lengths ranging from 3 to 101μm. The drain current of the short-channel TFT was saturated under V_{DS} = 5V with severe suppression of the current level in comparison with that of the long-channel TFTs. It should be noted that there is no s-shape behaviour for the low-VDS region in the output characteristics, indicating that the performance degradation of the short-channel a-IGZO TFTs with a-IZO S/D electrodes does not arise from the Schottky barrier dominant contact resistance, which is significantly affected by the value of V_{DS} in the

low-V_{DS} region.

In fact, the output characteristics of the short-channel TFT observed in this study can be also observed in TFTs with serially connected high parasitic resistance in S/D electrodes. Interestingly, the roll-over behaviour of I_{DS} can be observed only by increasing V_{DS} region. This behaviour can be explained when the saturation region mobility is much smaller than linear region mobility especially for the short-channel TFT. For a further analysis of the channel length dependent characteristics of a-IGZO TFTs, we extracted the field-effect mobility values in the linear and saturation regions as functions of V_{GS} and the channel length.

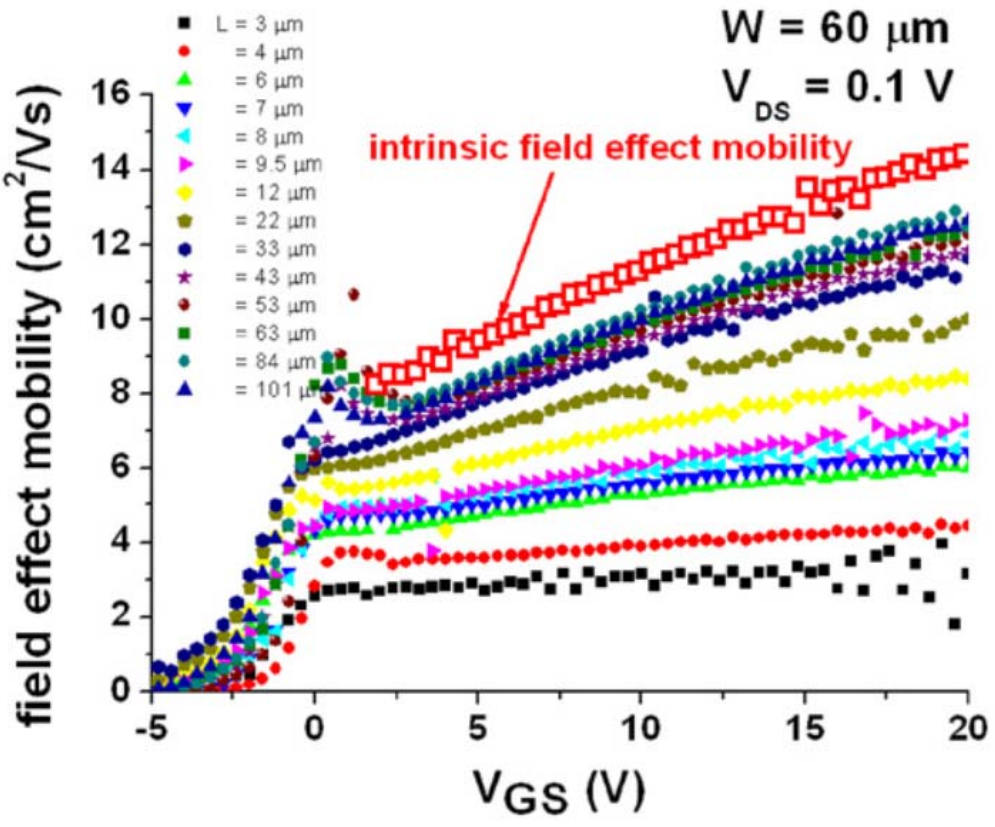

Figure 2-5. Field-effect mobility of a-IGZO TFTs as a function of V_{GS}.

The intrinsic field-effect mobility was extracted from the TLM results. Figure 2-5 shows the field-effect mobility (μ_{FE}) of a-IGZO TFTs in terms of V_{GS} in the linear region. The V_{GS} dependent field-effect mobility was extracted using the following equation:

$$\mu_{FE}(V_{GS}) = \frac{L}{C_{ins} W V_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}.$$

Here, C_{ins} is the gate insulator capacitance per unit area and W is the channel width. For the long-channel TFTs, the field-effect mobility values continuously increased as V_{GS} increased because the ratio of the free electron density in the conduction band edge compared with the trapped electron density increased, exhibiting behaviour similar to that of the intrinsic field-effect mobility extracted from the TLM as shown in figure 2-5.

However, for the short-channel a-IGZO TFTs, the field-effect mobility values remained constant up to large V_{GS} region indicating that the parasitic resistance is comparable to the channel resistance. If the parasitic resistance is increased further, the field-effect mobility may decrease for a large V_{GS} region, leading to severe non-linear behaviour of the transfer characteristics and field-effect mobility in the linear region. Figure 2-3(b) shows the field-effect mobility in the linear (μ_{FE} lin, V_{DS} = 0.1V) and saturation (μ_{FE} sat , V_{DS} = 20 V) regions. The mobility values were extracted from a linear regression plot of the transfer curves given as follows:

$$\mu_{FE\_lin} = \frac{L}{C_{ins} W V_{DS}} \frac{\delta I_{DS}}{\delta V_{GS}},$$

$$\mu_{FE\_sat} = \frac{2L}{C_{ins} W} \left(\frac{\delta \sqrt{I_{DS}}}{\delta V_{GS}} \right)^2.$$

In both regions, the field-effect mobility decreased as the channel length decreased due to the

increasing parasitic resistance effect. It is well known that the field-effect mobility of amorphous-based TFTs in the saturation region is larger than that in the linear region due to the V_{DS} dependent field-effect mobility arising from trap related Poole–Frenkel field emission. Accordingly, an increase in the field-effect mobility in the saturation region can be clearly observed for TFTs adopting low mobility semiconductor materials, such as a-Si:H and organic TFTs. However, we found that the field-effect mobility of a-IGZO TFT in the saturation region was lower than that in the linear region and it decreased further by about 1 $cm^2 V^{-1} s^{-1}$ especially when the channel length is short as shown in figure 2-6. The decrease in the field-effect mobility in the saturation region compared with that in the linear region was also observed in a-IGZO TFTs. This tells us that for the long channel TFTs whose electrical characteristics are independent of the parasitic resistance, the transport mechanism is not affected by the trap-related transport mechanism due to the low density of states and the high field-effect mobility.

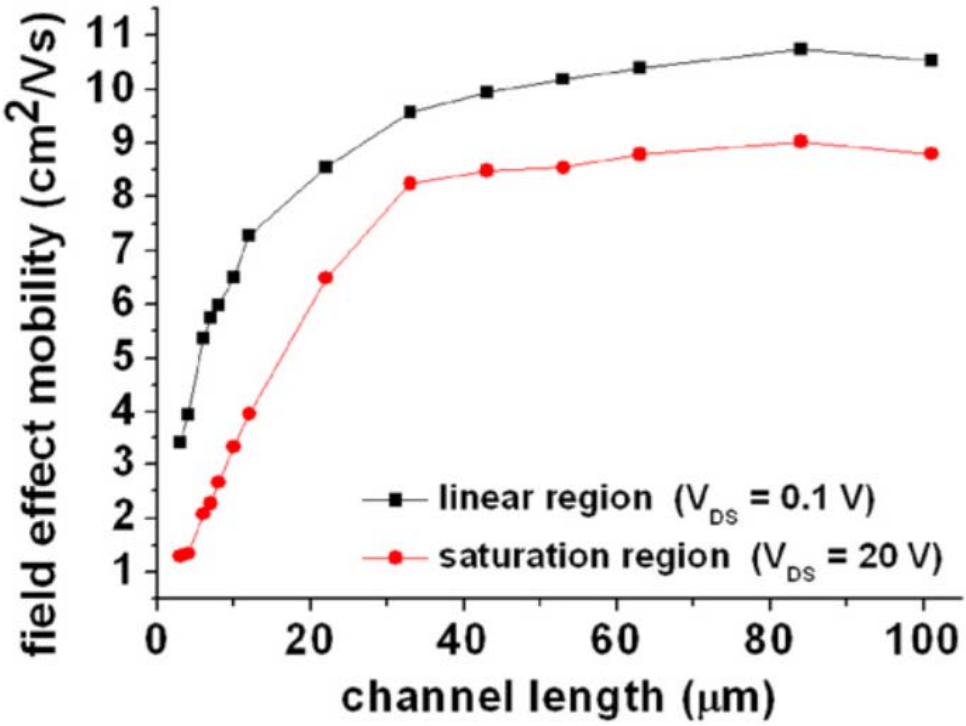

Figure 2-6. Field-effect mobility of a-IGZO TFTs in the linear and saturation regions as a function of the channel length.

We speculate that the severe decrease in field-effect mobility values in the saturation region for short-channel TFTs originated from sputtering damage during the deposition process of the a-IZO S/D electrodes. If the damaged region is slightly extended to the back-channel region, the decrease in the field-effect mobility becomes more severe in the saturation region, especially for the short-channel TFTs, because the bulk conduction through the back-channel region is dominant for high V_{DS}, leading to a decrease in the drain current at high V_{DS}, which is consistent with our case. This is also consistent with a previous report which found that even for the homo-junction formation between a-IZO semiconductor and a-IZO S/D electrodes, large parasitic resistance is induced by sputtering damage of a-IZO S/D electrodes.

The results can also be confirmed by TCAD simulation.

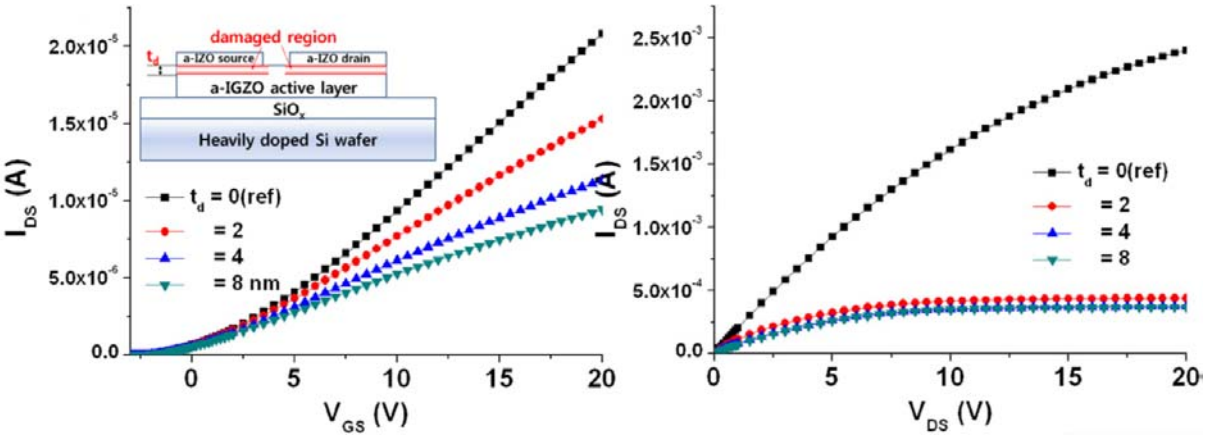

Figure 2-7. TCAD simulation results of (c) transfer (V_{DS} = 0.1V) and (d) output (V_{GS} = 20 V) characteristics for different t_d.

The severe decrease in drain current level can be observed for high V_{DS} condition. Figures 2-7 show transfer and output characteristics of a-IGZO TFT from TCAD simulation when low mobility regions (damaged region) are introduced in the back-channel region. Typical material parameters for the a-IGZO active layer were used, and the channel length and width were set to 3μm and 50μm, respectively. We assumed that the low mobility region is slightly extended into the back-channel region about 1μm from the edge of the S/D electrodes. The thickness of the low mobility region (td) was varied from 0 (reference) to 8 nm. The decrease in the drain current level for t_d = 2 nm was only 25% compared with the reference (t_d = 0 nm) at V_{GS} = 20V in linear region operation as shown in figure 3- 7(left). In contrast, there is severe decrease in drain current level, and early saturation behaviour of the output curves for high V_{DS} region when the damaged regions are introduced near the S/D electrodes as shown

in figure 2-7(right), which is consistent with our experimental results. This indicates that high performance and transparent short-channel TFT can be realized when the process conditions of the S/D electrodes are well optimized. To verify the parasitic resistance effect, we extracted the parasitic resistance ($R_{S/D}$) and current transfer length (L_T) values using TLM. The TFT total ON resistance (R_T) can be described in terms of the channel resistance and $R_{S/D}$,as follows:

$$R_T = r_{ch}L + R_{S/D} = L/[\mu_{FEi}C_{ins}W(V_{GS} - V_{THi})] + R_{S/D}.$$

Here, r_{ch} is the channel resistance per unit length, μ_{FEi} is the intrinsic field-effect mobility and V_{THi} is the intrinsic threshold voltage.

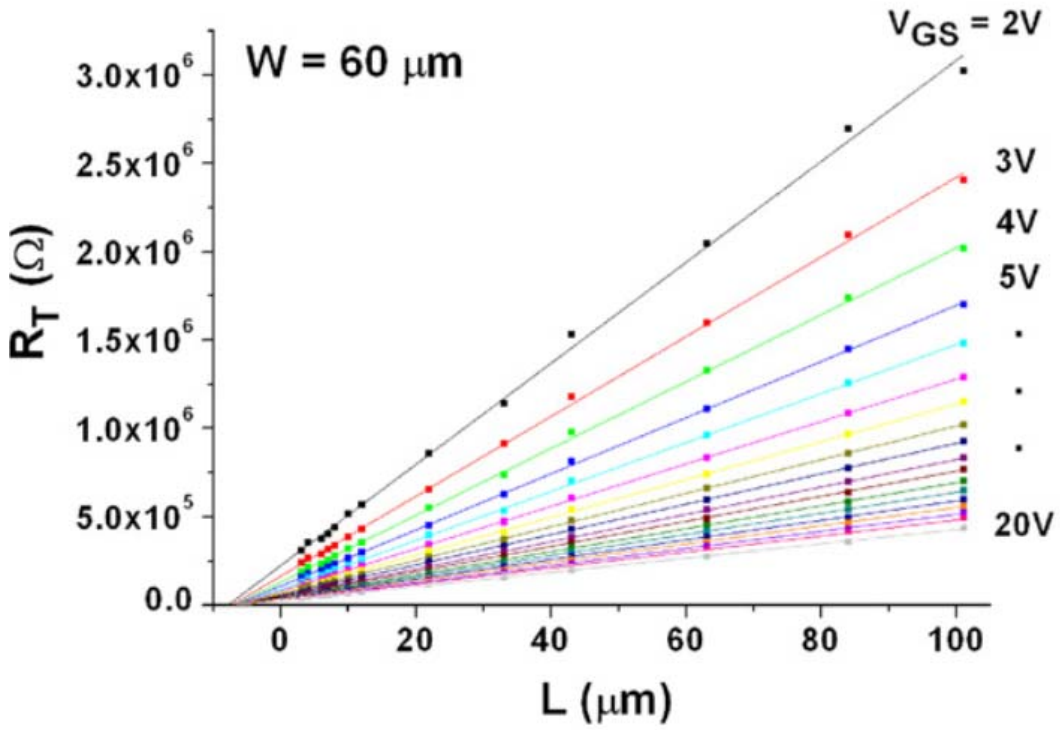

Figure 2-8. R_T versus L for different V_{GS} of a-IGZO TFTs. Solid lines denote the linear regression plot of R_T.

The measured data were fitted to linear regression plots. Figure 2-8 shows a R_T versus L plot for different V_{GS}. According to the linear regression plot (solid line) of R_T at a given V_{DS} (V_{DS} = 0.1V) for different V_{GS}, L_T and R_S/D can be obtained from the x and y intercept points, respectively. We assumed a resistive network model of parasitic resistance because there is no highly doped region under the S/D electrodes, unlike in a conventional MOSFET. In this case, LT has meaning when TFTs are operated in the accumulation state. Figure 2-9 shows the L_T and width-normalized parasitic resistance (R_p norm) values as a function of V_{GS}, respectively. The R_p norm was as high as 170 Ω cm at V_{GS} = 20V. In addition, L_T is much larger than that of conventional a-Si:H TFTs (~1 μ m); this is related to the maximally transferred current length, where the current level drops to 1/e in the channel region.

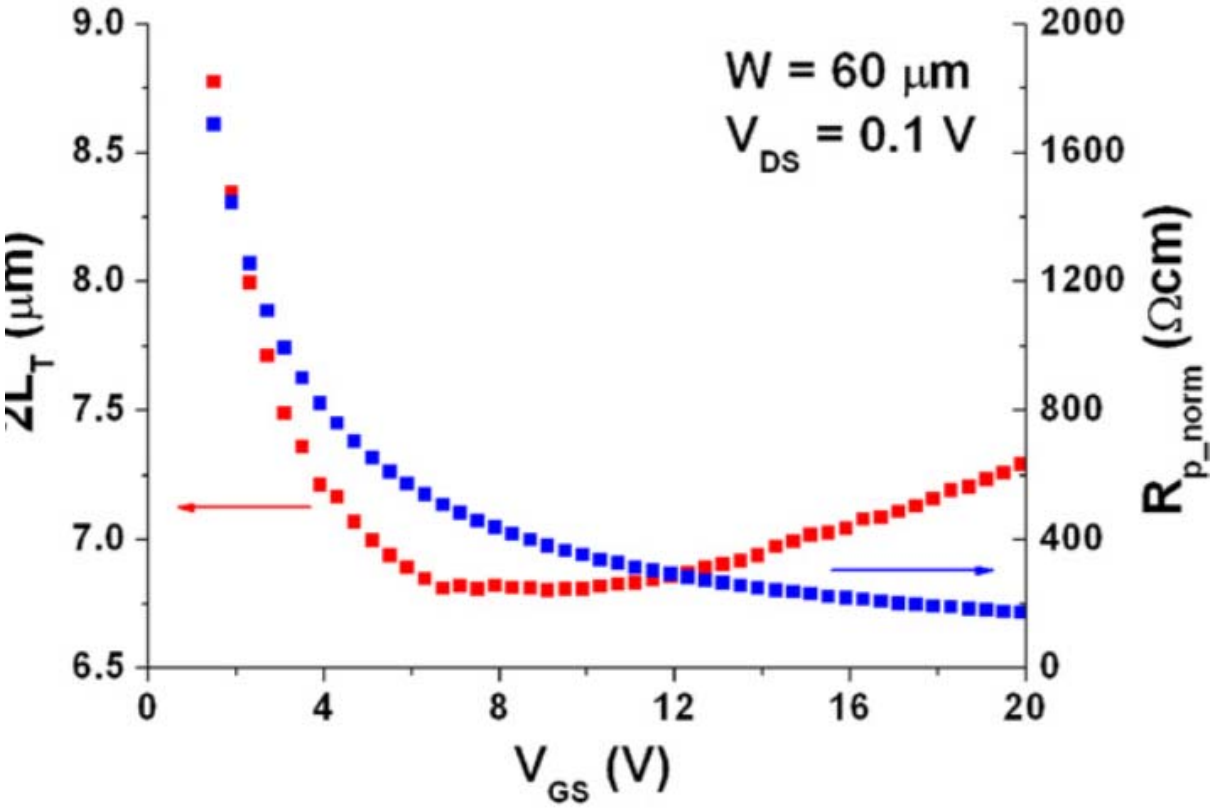

Figure 2-9. Current transfer length and width-normalized parasitic resistance as a function of V_{GS}.

This can be used to determine the gate overlap distance of TFTs with an inverted staggered bottom gate structure. Because the current transfer length is proportional to $\rho_c/r_{ch}W$, where ρ_c is the specific contact resistance, L_T increase as the field-effect mobility and parasitic resistance increases. Accordingly, the considerable parasitic resistance and the high field-effect mobility can be the origin of the long current transfer length. Given that the gate overlap distance is larger than $2L_T$, a long gate overlap distance larger than 7μm is required for a-IGZO TFTs with transparent a- IZO S/D electrodes. This also indicates that scaling down of a-IGZO TFTs with transparent a-IZO S/D electrodes is difficult because the effective channel length becomes much larger than the mask channel length due to the sputtering damage that arises during the a-IZO S/D deposition process. Therefore, an additional process for the S/D contact region is essential to reduce S/D parasitic resistance and achieve scaling down of the a-IGZO TFTs with a-IZO transparent S/D electrodes.

We analysed the scaling behaviour of a-IGZO TFTs with a-IZO transparent S/D electrodes. A decrease in field-effect mobility in the saturation region as compared with that in the linear region was found to have originated from sputtering damage that occurred during the a-IZO S/D electrodes deposition process. This becomes more prominent when the channel length is short. This also induced large parasitic resistance and a long gate overlap distance due to the long current transfer length, indicating that control of the parasitic resistance is essential for

the scaling down of a-IGZO TFTs with transparent a-IZO S/D electrodes.

2.3 Temperature effect of a-IGZO TFTs

In this chapter, we studied the intrinsic properties of a-IGZO TFTs with amorphous indium-zinc-oxide (a-IZO) source/drain (S/D) electrodes using temperature-dependent current-voltage and GFP measurements. We extracted various intrinsic parameters, such as intrinsic field-effect mobility and parasitic resistance in S/D electrodes, and analyzed their relationship using the GFP measurements.

A-IGZO TFTs were fabricated on a heavily doped n-type silicon substrate which was used as a substrate and a back gate. A radio-frequency magnetron sputtering system and a direct-current magnetron sputtering system were used to deposit an a-IGZO active layer (thickness=50 nm) and a-IZO S/D electrodes (thickness=100 nm). A conventional photolithography method and a wet-etching process were used to pattern the layers. A thermal annealing process in oxygen ambient was performed before the deposition of the a-IZO S/D electrodes to minimize the annealing effect in S/ D contact region. To improve the bias stress stability, the fabricated samples were stored in a vacuum for more than one month. The a-IGZO TFTs had very good bias stress stability without any passivation layer. The temperature-dependent measurements were performed at temperatures ranging from 93K to 373K in a low vacuum condition ($<5 \times 10^{-3}$ Torr). The low temperature measurement (<room temperature) was performed using a sample stage embedding a liquid nitrogen circulation system. Since the silicon substrate has good thermal conductivity, it can be assumed that the temperature differ-

ence between the sample and the stage was negligible.

2.3.1 Temperature-dependent current-voltage characteristics

Figure 2-10(a) shows the transfer characteristics of a-IGZO TFTs for different temperatures ranging from 93 to 373 K. At a low temperature range, the variation of the transfer characteristics was negligibly small from about 93 to 253 K.

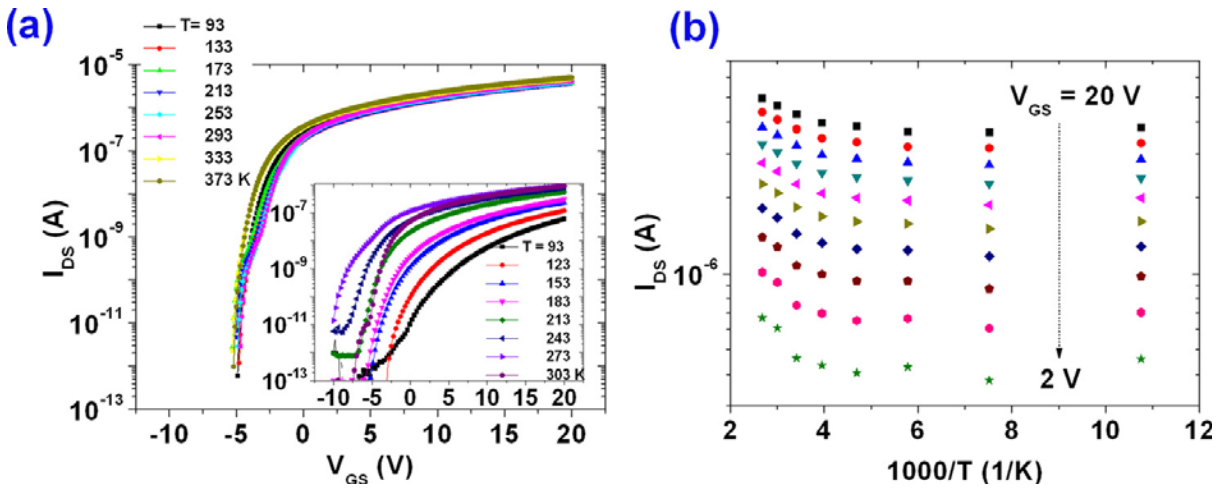

Figure 2-10. (a) Transfer characteristics of a-IGZO TFTs for different temperatures in a vacuum (main panel) and in ambient air (inset). (b) Arrhenius plot of IDS for different values of V_{GS}.

No thermally activated behavior was observed at this low temperature range. Slight thermal activation of the drain current can be observed only at a high temperature range. This is confirmed from the Arrhenius plot of the transfer curve as shown in Fig. 2-10(b), which is differ-

ent not only from that of a crystalline metal-oxide semiconductor field-effect transistor (c-MOSFET) but also from those of conventional amorphous based TFTs, such as organic TFTs and a-Si:H TFTs. We found that reducing the moisture in the act region is a key factor to obtain temperature-independent transfer characteristics in a-IGZO TFT as shown in the inset f Fig. 2-10(a), because significantly thermally activated behavior was observed when the low-temperature measurement was performed in ambient air containing a large amount of moisture. For this measurement, we used a-IGZO TFT with 100 nm-thick aluminum S/D electrodes. Given that our GFP patterned a-IGZO TFTs with a-IZO S/D electrodes were stored in a vacuum for a long time to sufficiently diffuse out redundant moisture, the moisture effect can be ignored when the measurement is performed in a vacuum as shown in the main panel of Fig. 2-10(a). It is known that the drain current shows thermally activated behavior when electrons trapped in defect sites are thermally activated to conduction band edge in amorphous based TFTs. In this case, the electron transport is governed by trap limited conduction. However, in our case, a conventional trap related transport mechanism cannot be applied to explain nearly temperature independent characteristics at a low temperature range. This is due to a significant low defect density of states of the a-IGZO TFTs in the sub-bandgap region. The similar temperature independency of threshold voltage shift of a-IGZO TFTs with the low defect density of states has been reported by theoretical analysis of defect states, which is in good agreement with our case. On the contrary, the slight temperature dependency of the drain current at the high temperature region can be attributed to the percolation of electron transport in the conduction band edge. It is well known that oxygen vacancies are

created when the temperature increases leading to an increase in the electron density in the active region.

The increase in the electron density induces an increase in the percolation conduction probability and in the drain current. In our case, the increase in the drain current corresponding to the creation of oxygen vacancies was mainly observed at a high temperature region with a slight negative shift of threshold voltage, as shown in Figs. 2-10(a) and 10(b). We speculate there is a threshold point to freeze-out the formation of oxygen vacancies because the increase in the drain current was accelerated at a high temperature region. Depending on the barrier height, barrier distribution, and carrier density, the percolation of electron current path yields the increase in the Hall mobility for increasing temperature especially when the carrier density is low, resulting in the increase in the drain current of a-IGZO TFTs. If the Hall mobility increases as the temperature increases, the parasitic resistance can decrease, which also induces the increase in drain current if the access parasitic resistance in the bulk region is a dominant factor. Therefore, to further verify the origin of the increase in the drain current, separate analysis of the intrinsic field-effect mobility and the parasitic resistance as a function of the temperature are essential for an accurate characterization of the temperature-dependent behaviors of a-IGZO TFTs.

2.3.2 Temperature-dependent parameter extraction using a GFP method

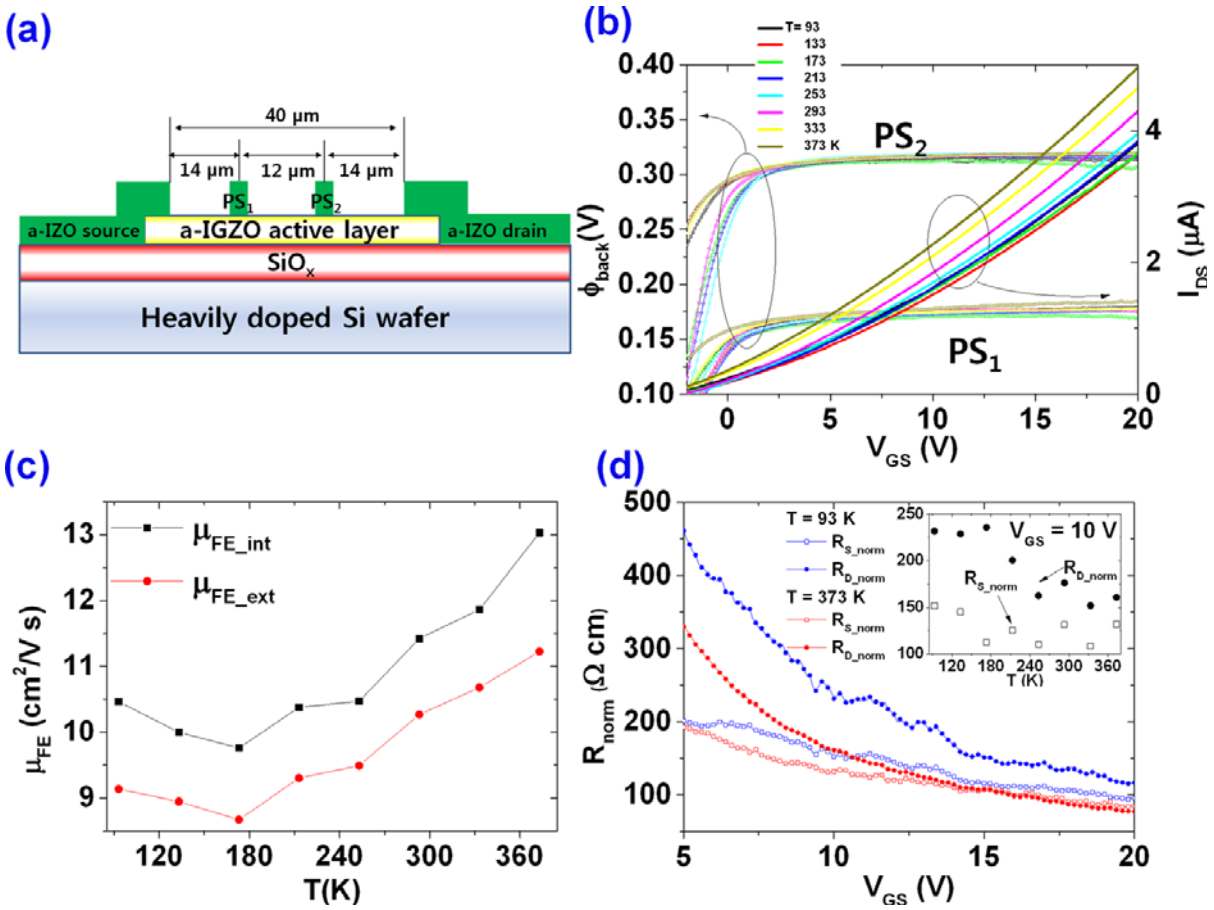

Figure 2-11. (a) A schematic diagram of the GFP patterned a-IGZO TFT; (b) GFP measurements of a-IGZO TFTs at different temperatures (V_{DS}=0.5 V); (c) resulting width-normalized parasitic resistance as a function of V_{GS} for different temperatures; (d) intrinsic and extrinsic field-effect mobility values as a function of the temperature.

The parasitic resistance and the field-effect mobility values were then extracted using a GFP method with V_{GS} ranging from 5 to 20V (V_{DS}=0.5 V) to analyze the origin of the increase in the drain current. A schematic diagram of a GFP-patterned a-IGZO TFT is shown in Fig. 2-11(a). The distances between each electrode were accurately measured by an optical micro-

scope. Figure 2-11(b) shows the measured back channel potentials (ϕ_{back}) at probing sites (PS) 1 and 2. When V_{GS} decreases from positive to negative values, the electron channel of TFTs transits from a strong accumulation state to weak accumulation or depletion states and the back channel potential begins to be affected by V_{GS} in both sides of the electrodes. The parasitic resistance and the intrinsic field-effect mobility values can be extracted in the strong accumulation region. Under this condition, the variation of the back channel potential was small as the temperature varied, as shown in Fig. 2-11(b). A slight increase in the back channel potential was observed only on the source-side electrode. The intrinsic and extrinsic field-effect mobility values (μ_{FEi} and μ_{FEe}) were calculated using the GFP method and the conventional extracting method of field-effect mobility in the VGS ranging from 5 to 20V, which are given as

$$\mu_{FEi}(V_{GS}) = \frac{(X_{PS2} - X_{PS1})}{C_{ins}W(V_{PS2} - V_{PS1})}\frac{\Delta I_{DS}}{\Delta V_{GS}},$$

$$\mu_{FEe}(V_{GS}) = \frac{L}{C_{ins}WV_{DS}}\frac{\Delta I_{DS}}{\Delta V_{GS}}.$$

Here, C_{ins} is the capacitance of the gate insulator, X_{PS1} and X_{PS2} are the distances of probing sites 1 and 2 as measured from the source side, and L is the channel length. Since the back channel potential is nearly constant in the strong accumulation state, V_{PS2} - V_{PS1} can be assumed as a constant value for different V_{GS}. Resulting intrinsic field-effect mobility values exhibit temperature-independent behavior at a low-temperature range whereas they show slightly thermally activated behavior at a high temperature range, thus showing a temperature dependency similar to the extrinsic field effect mobility, as shown in Fig. 2-11(c) with the drain current shown in Fig. 2-11(b). Because (μ_{FEi} and μ_{FEe})/ μ_{FEi} denotes the degree of

the parasitic resistance effect with a maximum value of about 15%, the parasitic resistance effect can be ignored in our a-IGZO TFT due to its sufficiently long channel length. Therefore, the slightly thermally activated behavior of the drain current in the high temperature region mainly stems from thermally activated intrinsic field-effect mobility, which is different from conventional amorphous based TFTs because the electron percolation in the conduction band is the dominant mechanism of the temperature-dependent Hall mobility in the a-IGZO TFTs. Figure 2-11(d) shows the resulting width (W)-normalized parasitic resistance for different V_{GS} values on the source (R_S, R_{S_norm} =W x R_S) and drain sides (R_D, R_{D_norm} =W x R_D) as calculated from the following equations:

$$R_s = \left(\frac{V_{PS1}X_{PS2} - V_{PS2}X_{PS1}}{X_{PS2} - X_{PS1}} \right) \frac{1}{I_{DS}},$$

$$R_d = \left[V_{DS} - \frac{L(V_{PS2} - V_{PS1}) + V_{PS1}X_{PS2} - V_{PS2}X_{PS1}}{X_{PS2} - X_{PS1}} \right] \frac{1}{I_{DS}}.$$

Asymmetric S/D contact resistances were obtained in a low V_{GS} region for different temperatures, as shown in the inset of Fig. 3-11(d). These may have originated from the non-uniform electrical characteristics of contact or bulk regions under S/D electrodes because we deposited the S/D electrodes after the thermal annealing process which can reduce the non-uniformity of the contact or bulk regions under the S/D electrodes. However, it should be noted that the contact resistance was not affected by Schottky barrier related thermionic emission because when $1/(R_{norm}T^2)=A\exp(-\phi_{br}/kT)$ (A is the proportional constant, ϕ_{br} is the barrier height of the Schottky junction, and k is the Boltzmann constant. The image force barrier lowering effect was not considered) is assumed at a given V_{GS}, negative values of ϕ_{br} which have no physical meaning were obtained for all temperature regions (not shown here).

In addition, a strong electric field-induced tunneling emission effect can be excluded in our case due to the low V_{DS} voltage. Instead, the $1/R_{norm}$ values show slightly thermally activated behavior.

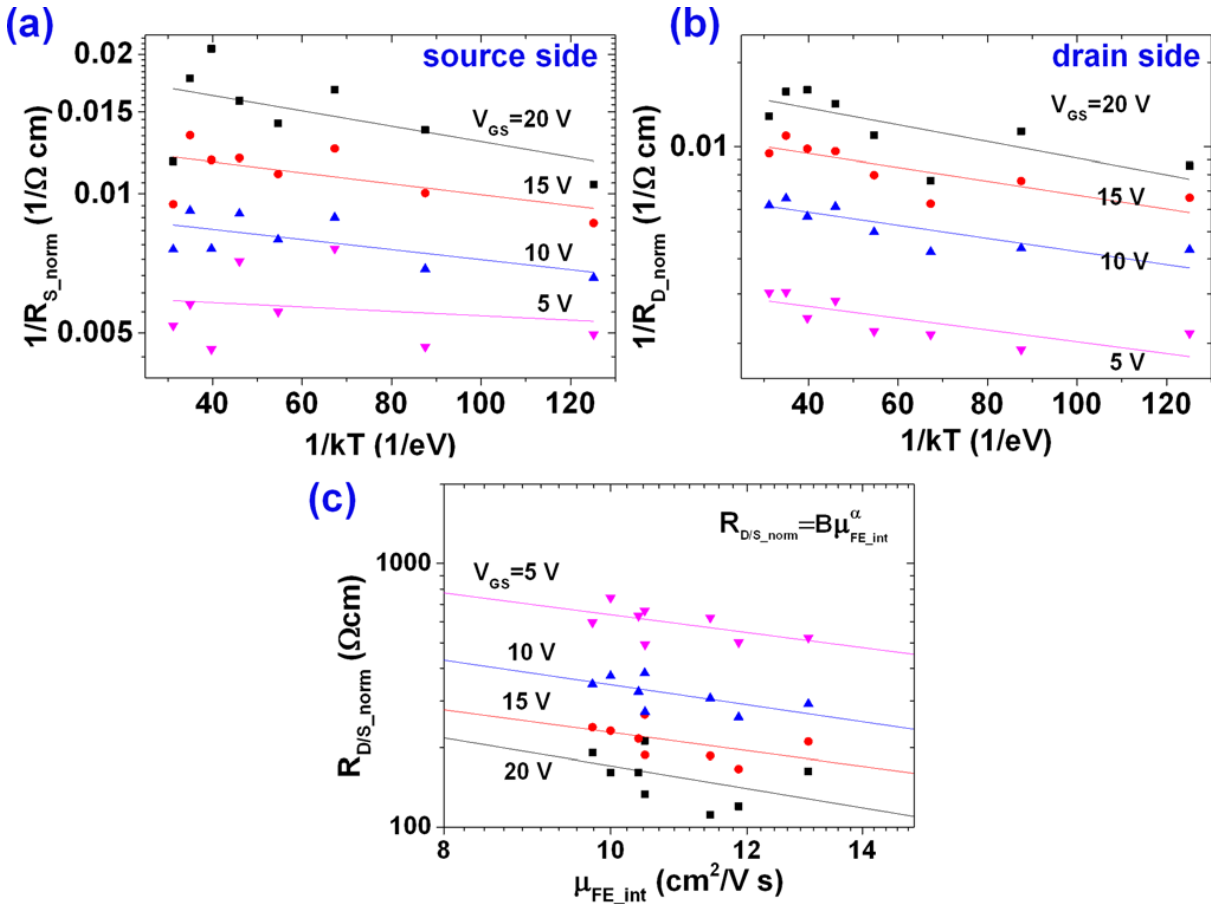

Figure 2-12. Arrhenius plots of $1/R_{D/S\_norm}$ for different values of V_{GS} on (a) source side and (b) drain side. (c) R_{D/S_norm} vs. μ_{FE_int} for different V_{GS} values.

Figures 2-12(a) and (b) show Arrhenius plots of $1/R_{norm}$ according to different temperatures on the source and drain sides, respectively. Assuming $1/R_{norm}=A\exp(-E_a/kT)$, where A is the proportional constant and E_a is the activation energy, the extracted E_a values were about 3.8, 2.7, and 2.5meV on the source side, while they were about 6.8, 5.7, 5.0, and 4.8meV on the

drain side, for V_{GS} = 20, 15, 10, and 5V, respectively. A fitting line on the source side for V_{GS}=5V was not considered due to a large standard error. Both the absolute values and the activation energy of the parasitic resistance on the source side are small in comparison with those on the drain side. However, these values are much smaller than those of a-Si:H and pentacene TFTs where the distribution of the defect density of states plays an important role in determining the contact characteristics. Therefore, based on the above discussion, neither defect-related transport nor Schottky barrier-limited transport dominantly influences the contact characteristics of a-IGZO TFTs. In this case, a possible origin of the parasitic resistance is the access resistance arising from the bulk region under the S/D electrodes. Figure 2-12(c) shows the relationship between the S/D parasitic resistance (R_{D/S_norm}) and μ_{FE_int} for different V_{GS}. The solid lines were fitted using a power law equation described as $R_{D/S\_norm}=B\ \mu_{FE\_int}^{\alpha}$, where B is the proportional constant and a is the exponent. Only rough estimations of the physical meaning of a values were considered due to large standard errors.

The extracted values of α were about -1.0, -0.87, -0.96, and -0.85 for V_{GS}=5, 10, 15, and 20V, respectively, indicating that there is a correlation between the intrinsic field-effect mobility and the parasitic resistance because the parasitic resistance decreases as the intrinsic field-effect mobility increases. This means that the parasitic resistance is a function of the intrinsic field-effect mobility or the Hall mobility, and the access parasitic resistance is the dominant factor to determine the contact characteristics of a-IGZO TFTs. Though a thermal annealing process was not applied after the deposition of the a-IZO S/D electrodes, the parasitic resistance was not affected by the band alignment and the distribution of the defect den-

sity of states between the a-IZO electrodes and the a-IGZO semiconductor layer, which differs from conventional amorphous based TFTs. It can be expected that the analysis of parasitic resistance used in this study plays an important role to characterize the electrical characteristics of a-IGZO TFTs, especially when the channel length is short due to an increased parasitic resistance effect for short channel length TFTs.

In conclusion, we analyzed the temperature-dependent electrical characteristics of a-IGZO TFTs using a GFP method. We found that the temperature dependency of the intrinsic field-effect mobility and the corresponding drain current level are closely related to the percolation conduction of electrons in the a-IGZO TFTs. As the temperature increases, the increase in the intrinsic field-effect mobility value results in a decrease in the parasitic resistance. The variation of the parasitic resistance is correlated with the variations of the bulk resistance under the S/D electrodes which is affected by the intrinsic field-effect mobility. Therefore, unlike conventional amorphous based TFTs, the metal/semiconductor barrier or the distribution of the defect density of states does not affect the contact characteristics of a-IGZO TFTs. Based on our results, further improvement in the performance of a-IGZO TFTs is possible by optimizing the various intrinsic characteristics.

2.4 Oxygen dispersive diffusion effect of a-IGZO TFTs

In this chapter, we studied V_{TH} instability in a-IGZO TFTs by varying the semiconductor layer (active layer) thickness from 6 to 100 nm. For a-IGZO TFTs with a thin active layer (t < 50 nm), we found that the oxygen diffusion has the greatest influence on the VTH instability. We fabricated a-IGZO TFTs on a thermal SiOx gate insulator (200 nm)/heavily doped n-type Si wafer, as shown in Fig. 2-13(a). First, a-IGZO (In : Ga : Zn = 1 : 1 : 1) semiconductor active layers [thickness (t) = 6, 10, 20, 50, and 100 nm] were formed by a radio frequency magnetron sputtering system. To reduce the inter-diffusion of the source/drain (S/D) electrodes during the annealing process, the active layers were annealed at 300° C for 1 h in an ambient oxygen environment before the deposition of the S/D electrodes. Then, a 200-nm-thick indium zinc oxide (IZO, In : Zn = 9 : 1) layer was sputtered by DC magnetron sputtering and patterned by a lift-off process. Figure 2-13(b) shows a cross-sectional transmission electron microscopy (TEM) image of a-IZO/a-IGZO/ SiOx layers when t = 6 nm. The variations of the measured active layer thicknesses were within 1 nm in comparison with the target thickness.

Figure 2-13(c) shows the initial transfer characteristics of a- IGZO TFTs with different thicknesses of the active layer. A negative shift of V_{TH}, an increase in the subthreshold slope (SS) value, and a decrease in the field-effect mobility value were observed when the active layer thickness was increased from 10 to 100 nm. Meanwhile, the 6-nm-thick a-IGZO TFT shows a low performance compared with TFTs when t = 10 nm. This deterioration in the perfor-

mance of the a-IGZO TFT with a very thin active layer was also observed by other groups and was explained in terms of the mean free path of the electrons and deep traps in the front channel.

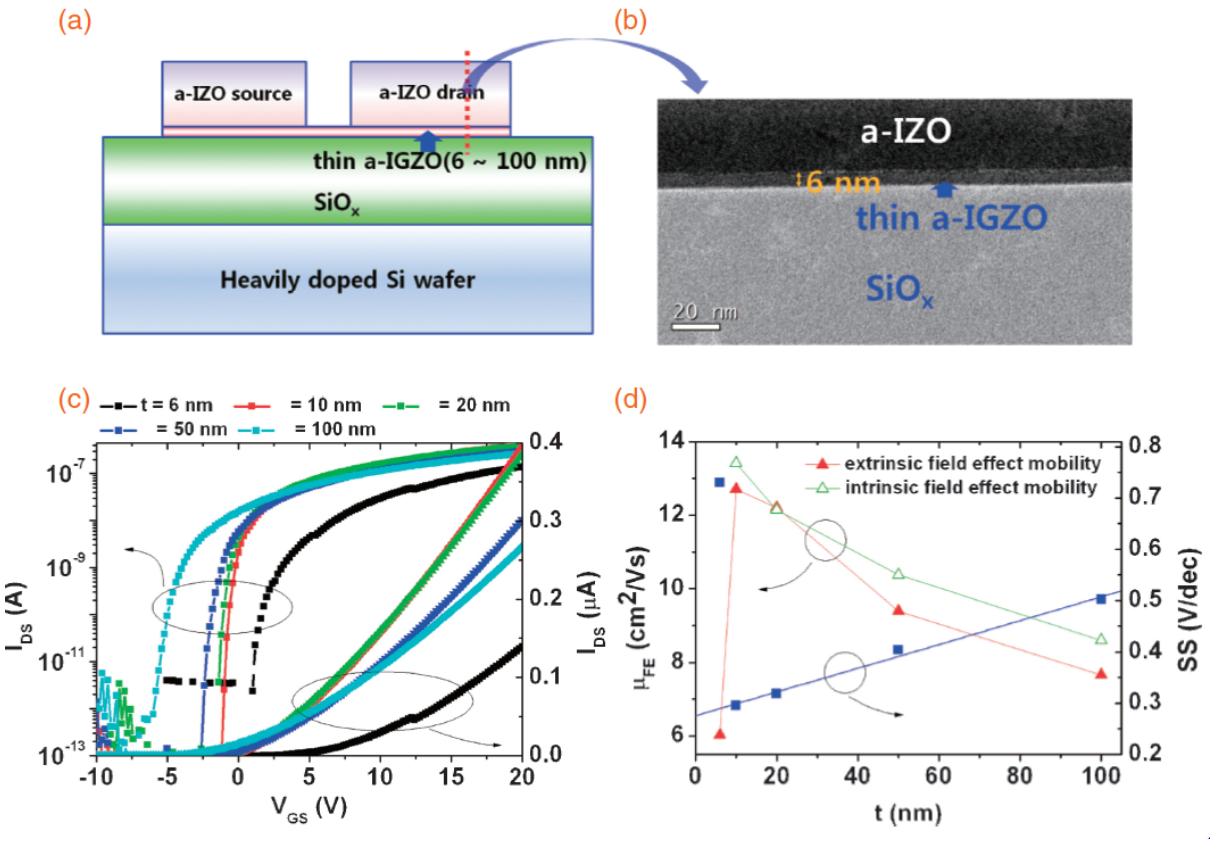

Figure 2-13. (a) Cross-sectional view of a-IGZO TFTs. (b) TEM image of a-IGZO TFT with t = 6 nm. (c) Initial transfer characteristics for different values of t. (d) Extracted field-effect mobility and subthreshold slope values as a function of active layer thickness.

Figure 2-13(d) shows a summary of the electrical characteristics as a function of the thickness of the active layer. The intrinsic field-effect mobility values were extracted by a transmission line method with the channel length ranging from 2 to 80um. The channel width was 60um. The TFTs show a distinct trend in the field-effect mobility values and in the SS values

except when t=6nm. It was noted that the decrease in the extrinsic field-effect mobility values originates from the decrease in the intrinsic field-effect mobility, which shows active layer thickness dependence similar to that in earlier results. The SS values show good linearity with respect to the active layer thickness when it ranges from 10 to 100nm. The interfacial trap density (D_{it}) and bulk trap density (N_{bt}) can be extracted using the following equation,

$$SS = (\log e)\frac{k_B T}{q}\left[1 + \frac{q^2}{C_{ox}}(D_{it} + tN_{bt})\right].$$

Here, k_B is the Boltzmann constant and C_{ox} is the capacitance of the gate insulator per unit area. The extracted values of D_{it} and N_{bt} were 3.7×10^{11} $cm^{-2}eV^{-1}$ and 4.0×10^{16} $cm^{-3}eV^{-1}$, respectively. From the initial electrical characteristics, the devices used in this study have similar interfacial and bulk defect densities for different active layer thicknesses owing to the thermal gate insulator layer having a low defect density of states. Accordingly, it can be assumed that V_{TH} instability does not depend on the active layer thickness if the charge trapping to the gate insulator layer is the dominant mechanism. The devices were subjected to prolonged V_{GS} stress for 3600 s (V_{GS}=20V). The transfer characteristics were measured every 100 s. Figures 2-14 (a) to (e) show the transfer characteristics for different active layer thicknesses and stress times. Positive shifts of V_{TH} were observed for all samples. However, the ΔV_{TH} values were initially increased and then became saturated (t $\geq$50nm) when the active layer thickness increased. Then, the samples were stored in vacuum for 34 days, and the same bias stress measurements were performed for all samples again. Figures 2-15 (a) and (b) show the transfer characteristics for t =6 and 10nm samples. Interestingly, all samples except when t =6nm show much stable operations under the same bias stress condition. These

behaviors cannot be explained by the typical charge trapping model which is widely accepted as one of the dominant mechanism of the instability of a-IGZO TFTs. Because the oxygen molecules are absorbed, and formed abundant interstitial oxygen states when the thermal annealing process is performed, the absorbed oxygen molecules can be diffused out when the samples are stored in the vacuum condition for a long time. This indicates that oxygen molecules play an important role to the instability of a-IGZO TFTs.

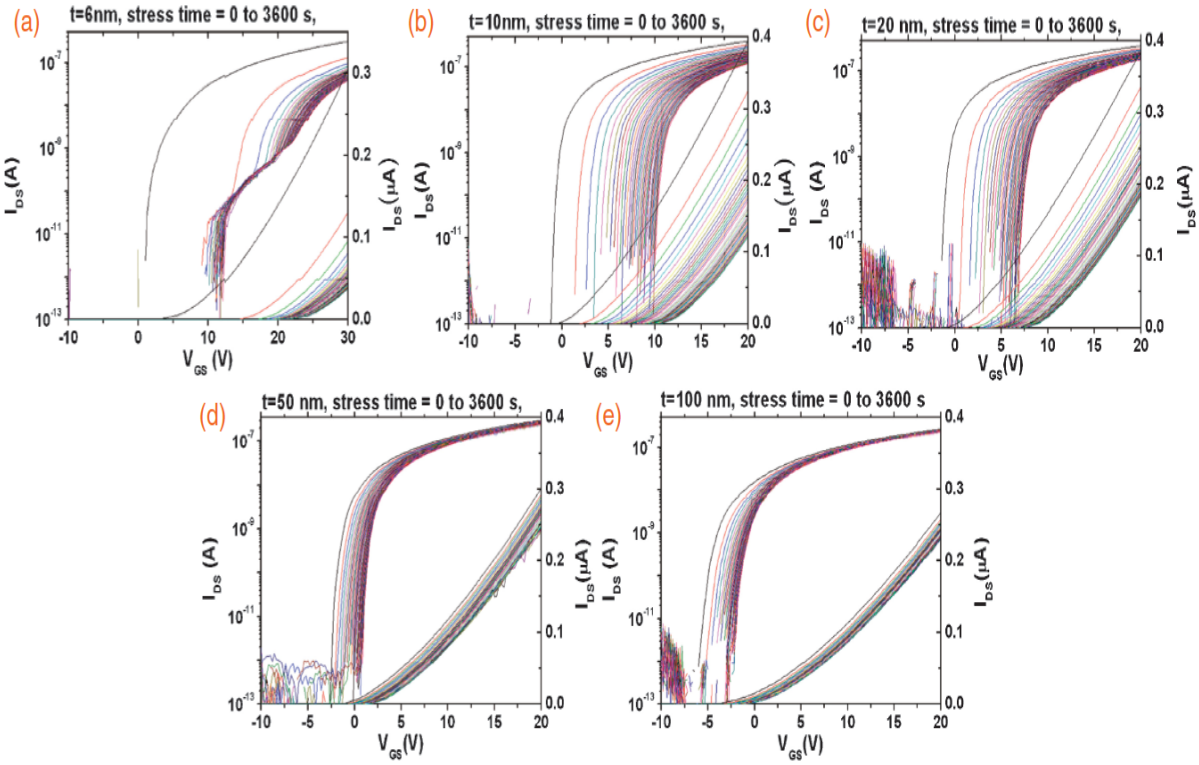

Figure 2-14. Evolutions of the transfer characteristics of a-IGZO TFTs during the stress measurement (V_{GS}=20V) for different values of t: (a) 6, (b) 10, (c) 20, (d) 50, and (e) 100 nm.

V_{GS} was swept from -10 to 30V for the TFT with t = 6 nm and from -10 to 20 V for the TFTs with t ≥ 10 nm.

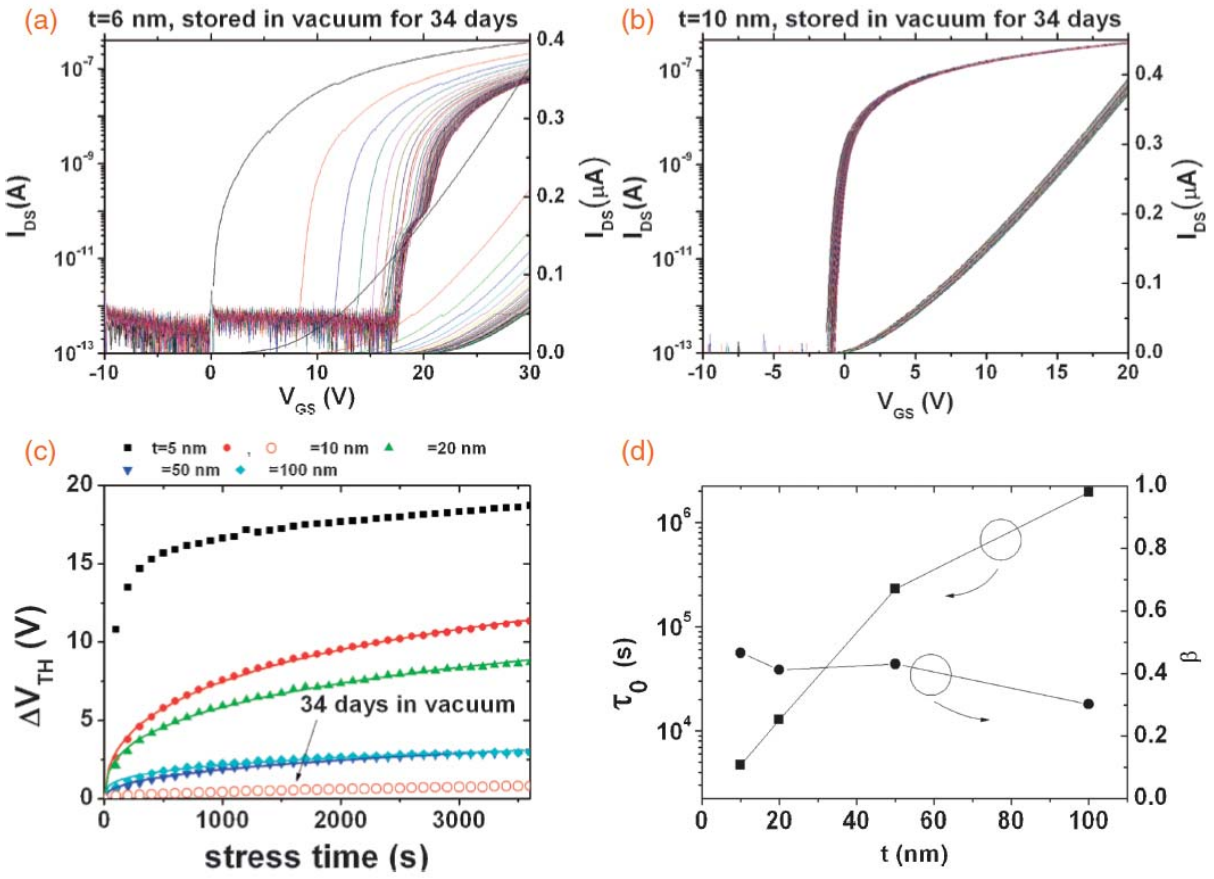

Figure 2-15. Evolutions of the transfer characteristics of a-IGZO TFTs stored in vacuum for 34 days for different values of t: (a) 6 and (b) 10 nm. (c) ΔV_{TH} vs stress time for different active layer thicknesses.

The solid lines are fitting lines using Eq. (4). (d) Extracted parameters of τ_0 and β as a function of the active layer thickness. Recently, Nomura et al. reported that an oxygen diffusion length is only 20 nm even at 400° C. Therefore, an oxygen-rich region can exist near a back channel region of the active layer if the annealing temperature is relatively low, which is 300° C in our case. Because it is well known that oxygen acts as an acceptor in an a-IGZO film and because the high electron density layer (channel layer) is thinner than the active layer under a high V_{GS} condition, the increase in the V_{TH} instability can be attributed to a de-

crease in the oxygen transfer length to the channel region through the active layer as the active layer thickness is decreased. In the case of t=6 nm sample, direct exposure to the ambient can greatly increase the instability even when the absorbed oxygen molecules are out-diffused, which will be further discussed later in this paper. Therefore, we speculated that the dispersive diffusion of oxygen from the oxygen-rich back channel region to the front channel region is the most probable origin of the V_{TH} instability of thin a-IGZO TFTs, which induces the creation of acceptor-like defect states in the sub-bandgap region.

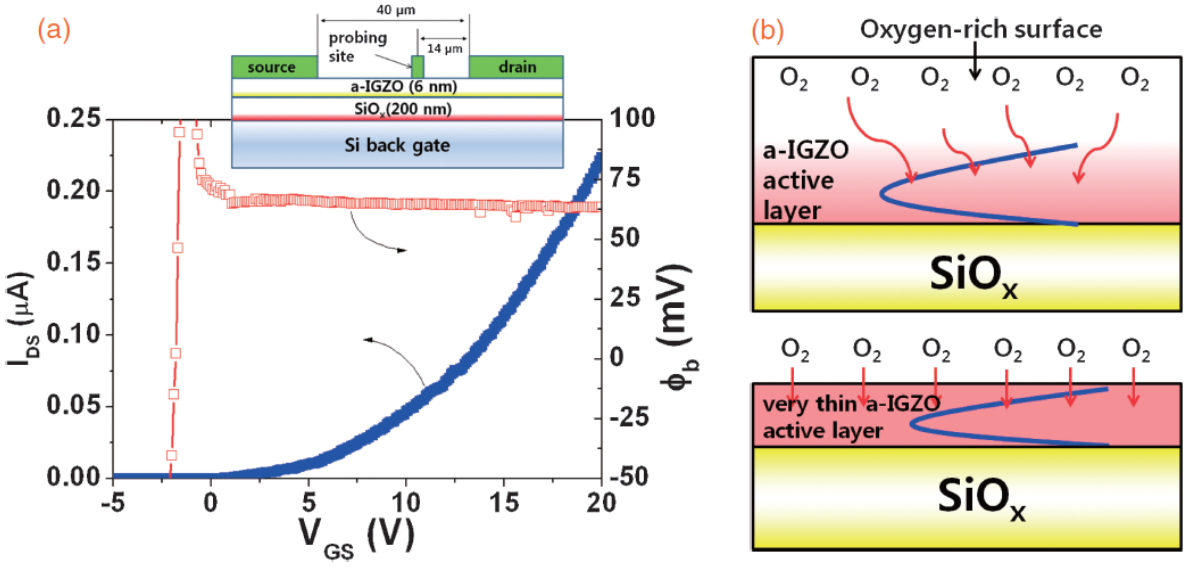

Figure 2-16. (a) Back channel potential as a function of V_{GS} measured by the GFP method. The inset shows the GFP structure used in this study. (b) Schematic diagram of the dynamics of an oxygen molecule for different thicknesses of a-IGZO active layers.

The blue curve denotes the quantum mechanical electron density distribution in the active layer. The creation of new acceptor-like states can be verified from the hump like behavior in

the transfer characteristic for the t = 6 nm sample, which exhibits a large positive V_{TH} shift as shown in Fig. 2-16(a). The subthreshold slope reflects the density of states distribution in the sub-bandgap region. If new states are created under the bias stress condition, the subthreshold slope value increases when both donor and acceptor-like states are created. However, if the new states are donor-like states, the V_{TH} shifts to negative direction, which is not consistent to our case. In fact, it is well known that the creation of acceptor-like states induces the increase of the subthreshold slope value and positive shift of V_{TH}, which is frequently observed in the a-Si:H TFT.

Therefore, the large increase in the number of acceptor-like defect states in the sub-bandgap region, which originated from the ionized oxygen, can explain both the large positive ΔV_{TH} and the hump like behavior in the subthreshold voltage region when prolonged stress is applied. It is questionable as to why the stretched exponential relationship still holds when oxygen diffusion becomes the dominant mechanism of the V_{TH} instability in a-IGZO TFTs.

In conventional a-Si:H TFTs, the stretched exponential relationship can be explained by the dynamics of the hydrogen dispersive diffusion. Based on the hydrogen diffusion model, if the oxygen diffusion model for a-IGZO TFTs is assumed in a similar way, oxygen dispersive diffusion can induce a stretched exponential relationship between ΔV_{TH} and stress time. In a thin active layer, the diffusion coefficient of oxygen follows a power law in time (t_s), in this case, $D = D_0 t_s^{-\alpha}$, where D is the diffusion coefficient and $\alpha = 1-\beta$ ($\beta = T/T_0$, T is the temperature and T_0 is the characteristic temperature of the conduction band tail states). Because the rate of formation of acceptor-like defect states is proportional to the diffusion coefficient and

electron density in the channel region (n_{ch}) under the strong accumulation condition, the following equation can be obtained,

$$\frac{dN_A}{dt} \sim n_{ch} D_0 t_s^{-\alpha} = C_{OX}(V_{GS} - V_{TH}) D_0 t_s^{-\alpha}.$$

By integrating Equation. with respect to t_s and using the relationship $C_{OX}\Delta V_{TH} = \Delta N_A$, we can obtain the conventional stretched exponential equation,

$$\Delta V_{TH} = (V_{GS} - V_{TH0})\left\{1 - \exp\left[-\left(\frac{t_s}{\tau_0}\right)^{\beta}\right]\right\}.$$

Here, V_{TH0} is the initial threshold voltage (V_{TH} at $t_s = 0$) and τ_0 is the characteristic time.

Figure 2-15(c) shows the relationship between ΔV_{TH} and the stress time while assuming that oxygen diffusion is the dominant mechanism, which is fitted very well, except when t = 6 nm. The overdriving voltage values (V_{GS} - V_{TH0}) of the samples were 14.9, 19.5, 19.8, 20.1, and 22.2V when t = 6 to 100 nm. For the TFT when t = 6 nm, since the ΔV_{TH} was larger than V_{GS} - V_{TH0}, the experimental data did not fitted. The extracted parameters are shown in Fig. 3-15(d). The β values that are related to the conduction band tail states were in the range of 0.47 to 0.3, and the corresponding k_BT_0 values ranged from 55 to 86 meV, which shows slight active layer thickness dependence. In contrast, τ_0 shows a significant active layer thickness dependence varying from 4.7×10^3 to 1.9×10^6 s. The increase in the τ_0 value as the active layer thickness increases suitably explains the relationship between oxygen diffusion and the V_{TH} shift because the τ_0 term includes the diffusion length from the front channel to the back channel region in the active layer. Figure 2-16(a) shows the back channel potential (ϕ_b) variation as measured by a gated four-probe (GFP) method for the sample with t = 6 nm (V_{DS} = 0.1 V; ϕ_b was measured at a back channel probing site where the channel

length was 40 um and the distance from the drain electrode to the probing site was 14 um. Even for the a-IGZO TFT with a very thin active layer, the back channel region is electrically disconnected from the front channel region because $d\phi_b = dV_{GS} = 0$ when the TFT is in a strong accumulation condition. This indicates that a possible driving force of oxygen transfer to the channel region is the diffusion caused by a population gradient from the back channel to the front channel region rather than field induction. In addition, the extreme V_{TH} instability for the t = 6 nm sample can be explained by the direct exposure of the channel region to ambient oxygen, as shown in Fig. 2-16(b). In quantum mechanics, the electron density distribution is like a sine wave whose peak is slightly shifted to the gate side by the electric field if the electrons are in an infinite potential well. In our case, a conduction band edge of SiO_x, a conduction band edge of a-IGZO, and a vacuum level are formed nearly infinite potential well due to large difference of energy levels between the well and barriers. For this reason, in the thin active layer, the distance from the front channel to the back channel region becomes very small, and the channel layer is almost directly exposed to the ambient oxygen leading to severe V_{TH} instability as shown in Fig. 2-16(b). In conclusion, it was found that thickness dependent bias stress instability and the stretched exponential relationship between ΔV_{TH} and the stress time can be feasibly explained in terms of oxygen dispersive diffusion absorbed near the back channel region during an annealing process and the accompanying creation of acceptor-like states for a-IGZO TFTs with a thin active layer. For the a-IGZO TFT with t = 6 nm, direct exposure of the channel layer to the ambient oxygen induces severe V_{TH} instability and hump like characteristics, thus confirming the role of oxygen and the creation of the ac-

ceptor-like defect states for prolonged V_{GS} stress.

III. BENDING EFFECT OF a-InGaZnO THIN FILM TRANSISTOR AND BIAS STRESS IN-STABILITY TEST

3.1. Introduction

Recently, high-performance amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) have attracted much attention in the various fields of large-area electronics, such as flexible displays, smart windows, and smart sensors due to their high field-effect mobility, low-power consumption and good bias stability. Next-generation displays toward flexible and transparent displays have also been intensively investigated using both conventional hydrogenated amorphous silicon (a-Si:H) and oxide-based semiconductor materials. In particular, to meet the requirements of transparency and flexibility at the same, a-IGZO TFTs are considered as a good candidate for switching or driving devices. Several groups have reported the electrical characteristics of transparent a-IGZO TFTs on plastic substrates, such as polyethylene naphthalate (PEN) and polyethylene terephthalate (PET) for flexible or rollable display applications using a low-temperature process. However, the low-temperature process for an a-IGZO active layer decreases the performance of the a-IGZO TFT including field-effect mobility and bias stress stability, which reduce the merits of oxide-based TFTs. For high-temperature annealing process, polyimide (PI) substrates are frequently used for fabrication of the a-IGZO TFTs, which cannot be applied to transparent display applications due to the inherent yellowish color of the PI substrates. In addition, to achieve high transparency, high performance and good bias stress stability, a high-temperature thermal annealing pro-

cess on a transparent substrate is essential during the fabrication process. Meanwhile, leading display companies have begun research for curved organic light-emitting diode television which can increase the visibility from various viewing positions. Though the minimum bending radius of these types of display is relatively large in comparison with that of conventional flexible or stretchable devices, it can be expected that slight decreases in the bending radius using thin glass greatly increases the visibility of the display. For a 'slightly curved display', oxide based TFTs can be a good candidate for next-generation switching or driving devices.

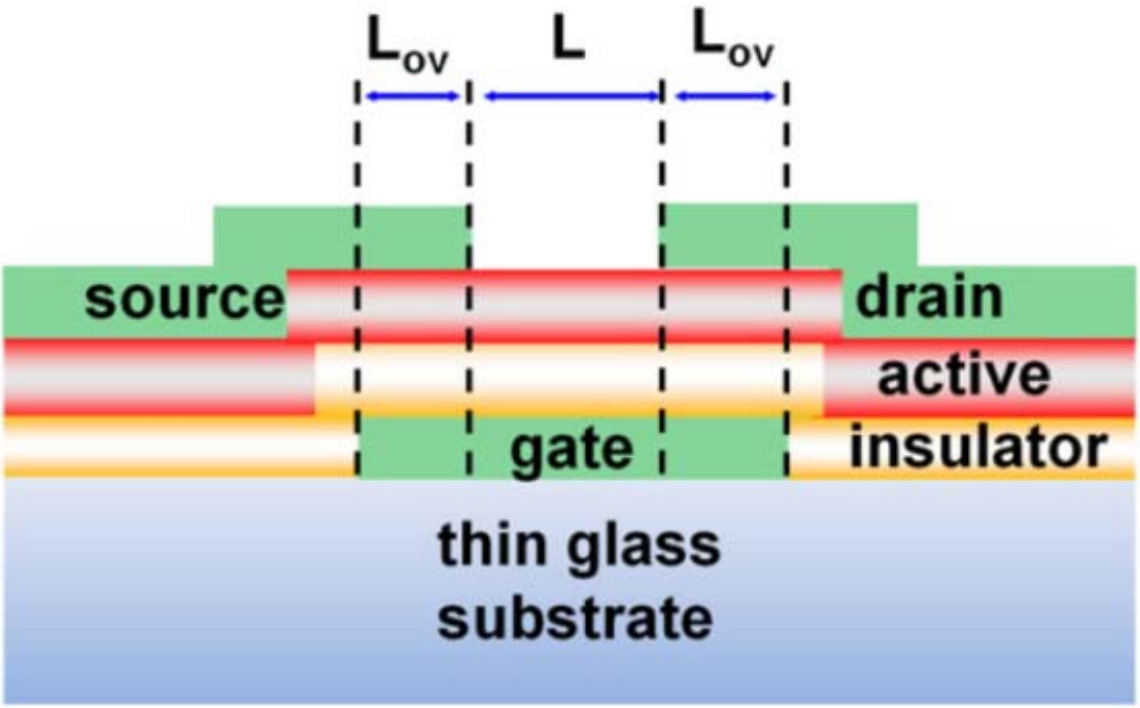

Figure 3-1. Drawing of cross-sectional view of a-IGZO TFT structure.

We demonstrated transparent and flexible a-IGZO TFTs on a thin glass substrate for slightly curved electronic application. Prolonged gate bias stress tests were performed under the flat and bending condition to ensure the stable operation of a-IGZO TFTs on thin glass substrate

for various conditions. We also fabricated depletion and enhancement load type inverters to elucidate the feasibility of a-IGZO TFTs on the thin glass substrate. A 70 μm-thick ultra-thin glass (D-263 borosilicate) substrate purchased from Schott was used as a flexible substrate. First, a thin glass substrate was attached to a silicon master wafer, and then cleaned by acetone, methanol and deionized water, sequentially. Then, a 100 nm-thick amorphous indium zinc oxide (a-IZO, In_2O_3 : ZnO = 90 : 10 wt%) layer was deposited using a direct current (dc) magnetron sputtering system. The gate electrodes were patterned by a photolithography and a wet etching process. After that, a 200 nm-thick SiNx layer was deposited using a plasma enhanced chemical vapor deposition process at 350 ◦C. Then, 80 nm-thick a-IGZO active film was sputtered by a radio frequency magnetron sputtering system (In:Ga:Zn = 1:1:1 in atomic ratio). Active islands were patterned by a photolithography method and a wet etching process. The thermal annealing process was performed for improvement of a-IGZO TFT performance and device stability in an oxygen ambient at 300 ◦C for 1 h. After that, gate via was formed by a photolithography and a reactive ion etching method. Finally, a 100 nm-thick a-IZO layer was deposited using a dc magnetron sputtering system and patterned by a lift-off process.

3.2 a-IGZO TFT on thin glass substrate

Cross-section and top view images of the a-IGZO TFT on the thin glass substrate are shown in figure 3-1. Figure 3-3 shows optical transmission spectra of the a-IGZO TFT on the thin glass substrate. The optical transparency of the a-IGZO TFTs was larger than 80% in visible wavelength ranging from 390 to 750 nm. Figure 3-2 is an optical microscope image of a fully transparent and flexible a-IGZO TFT on a thin glass substrate.

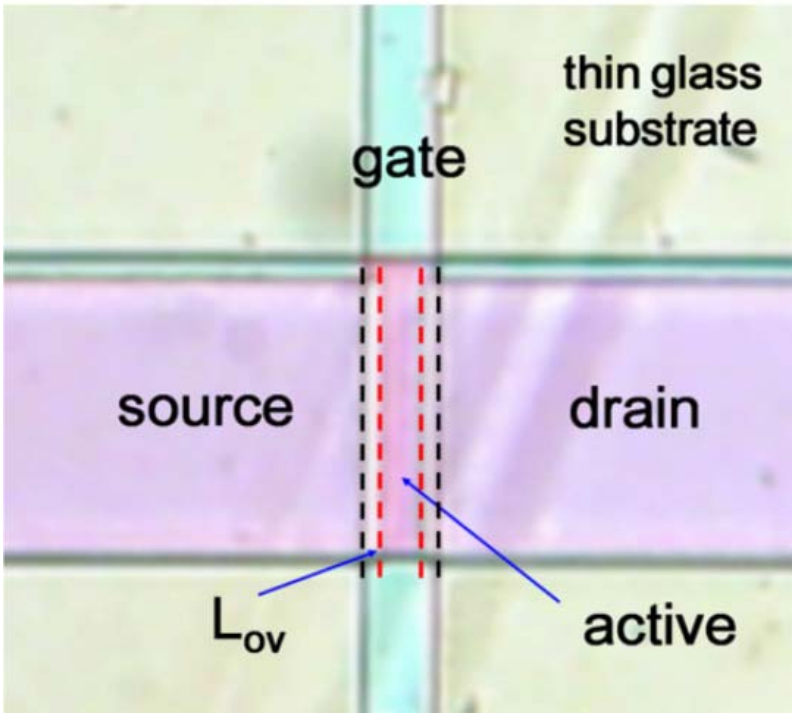

Figure 3-2. An optical microscope image of the a-IGZO TFTs on the thin glass substrate.

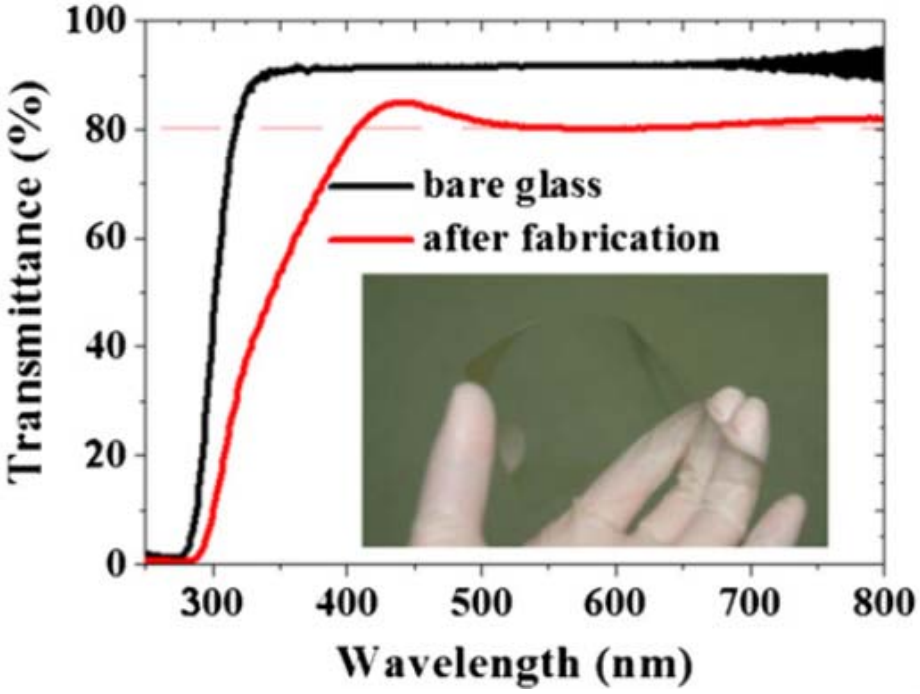

Figure 3-3. Transmittance versus wavelength measured by UV-visible spectroscopy.

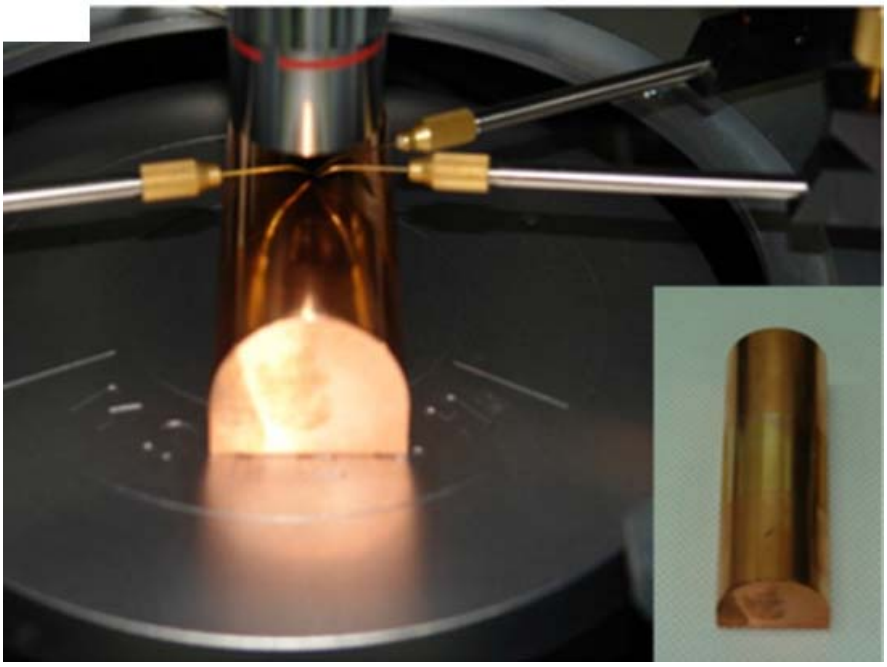

Figure 3-4. Photograph of I–V measurement tool. Inset is a curvature mold used for bending strain.

Two types of a-IGZO TFTs were fabricated, which have different gate overlap length (L_{OV}). One has symmetric gate overlap length with L_{OV} = 3 μm (S sample) and the other has asymmetric gate overlap length with L_{OV} = 0 and −8 μm for source and drain sides, respectively (AS sample). The negative sign of L_{OV} denotes that a high parasitic resistance bulk region with a length of 8 μm length was inserted between a channel region and a contact region. The AS samples were used to characterize the variation of parasitic resistance according to the variation of bending radius, and to analyze its effect on the variation of TFT electrical characteristics as a function of bending radius.

Table 3-1. Summary of electrical characteristics of S and AS samples before and after bending.

Sample ID	μ_{FE_lin} ($R\infty$, $cm^2\ V^{-1}\ s^{-1}$)	V_{th} ($R\infty$, V)	SS ($R\infty$, $mV\ dec^{-1}$)	ΔV_{th} ($R\infty$-$R4$)	ΔSS ($R\infty$-$R4$)
S	9.1	−5.4	858	−5.38	255
AS	3.1	−2.8	281	−0.25	8

3.3 Characteristics of symmetry and asymmetry in a-IGZO active

Transfer characteristics of the a-IGZO TFTs were measured in a substrate-flat-condition (R ∞). Figures 3-5, and 3-6 show transfer and output characteristics of S and AS samples. Initial TFT characteristics are summarized in table 3-1. We obtained superior electrical performance of the a-IGZO TFTs on the thin glass substrate compared to those on transparent polymer substrates. In particular, the a-IGZO TFT shows a high field-effect mobility up to 9.1 $cm^2\ V^{-1}$

s^{-1} and a high on/off current ratio larger than 10^8 A/A for the S sample as shown in table 3-1, which is comparable with those on the thick glass substrate. Meanwhile, the AS sample shows relatively poor electrical performance with a field-effect mobility value of 3.1 cm^2 V^{-1} s^{-1} due to a large parasitic resistance effect originated from the high resistance bulk region. However, the field-effect mobility of the AS sample is still larger than conventional low-temperature processed a-IGZO TFTs on a plastic substrate. The bending test of a-IGZO TFTs on the thin glass substrate was performed using semicircular shaped curvature molds as shown in figure 3-4. The bending radius was set to 50mm(R5) and 40mm(R4) by considering minimum bending radius before rupture of the substrate. The corresponding tensile strain values were 0.07% and 0.09% for R5 and R4 conditions, respectively.

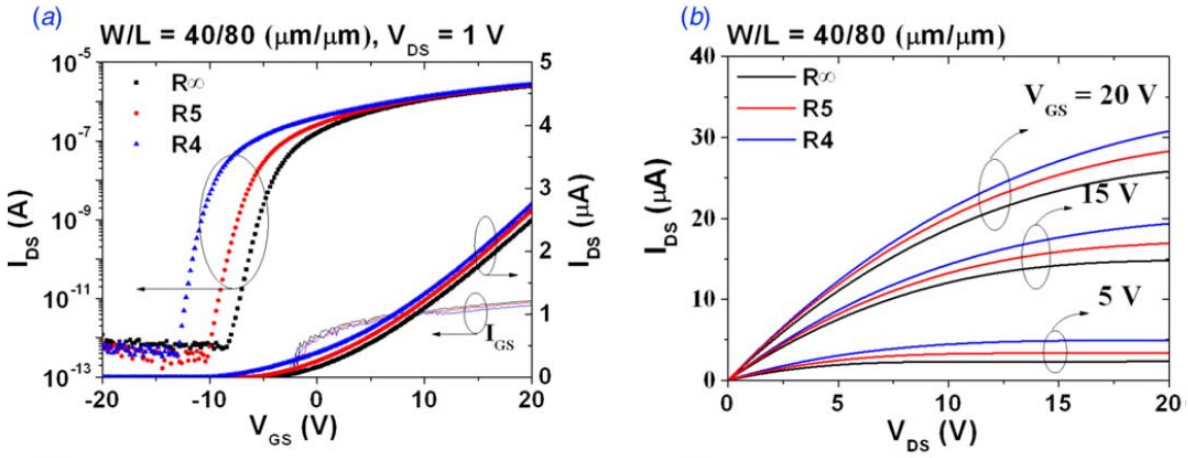

Figure 3-5. Transfer and output characteristics of S ((a) and (b)) samples.

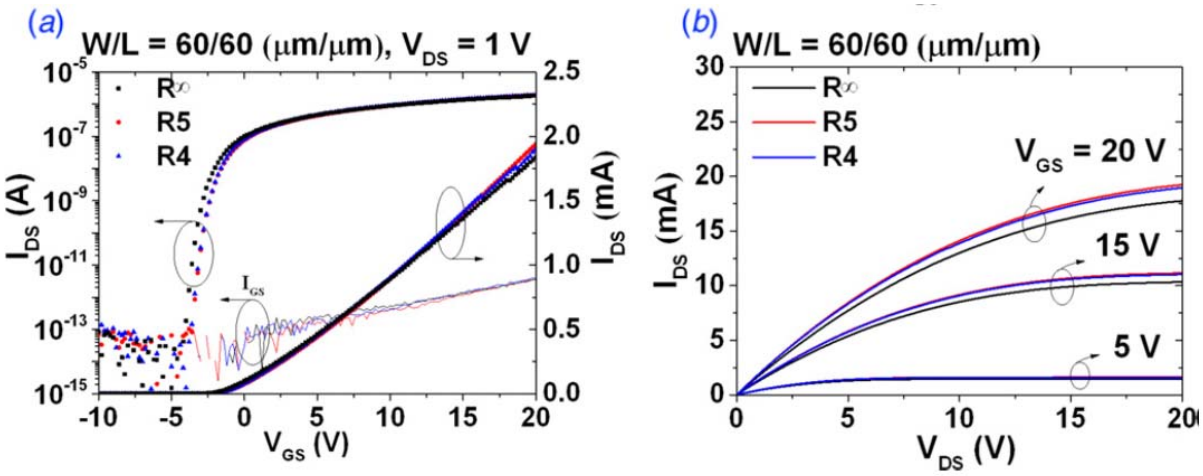

Figure 3-6. Transfer and output characteristics of AS ((a) and (b)) samples.

3.4 Bending effect of a-IGZO active

Bending direction was perpendicular to the channel current flow direction. The variations in transfer and output characteristics are also shown in figures 3-5 for R∞, R5, and R4 conditions. For the S sample, as bending radius and strain increased, a negative shift of threshold voltage (V_{TH}) was observed with an increase in the subthreshold slope (SS) and an increase in the drain current in output characteristic, as shown in figures 3-5. It is well known that application of tensile strain induces negative shift of V_{TH} for a-IGZO TFTs due to the creation of oxygen vacancies coming from low formation energy of oxygen vacancies which act as donor-like states. However, for the AS sample, the variations in electrical characteristics including V_{TH} shift and SS is relatively smaller than those of the S sample, as shown in figures 3-6 and as summarized in table 3-1. This is possibly due to the effect of the bulk region when the characteristics of the bulk region predominantly affect the TFT performance variations.

Accordingly, there are optimum conditions of device structure for stable operation of a-IGZO TFTs against the mechanical bending, though the field-effect mobility value becomes relatively low due to large parasitic resistance for the AS sample.

3.5 Depletion and enhancement load type inverters

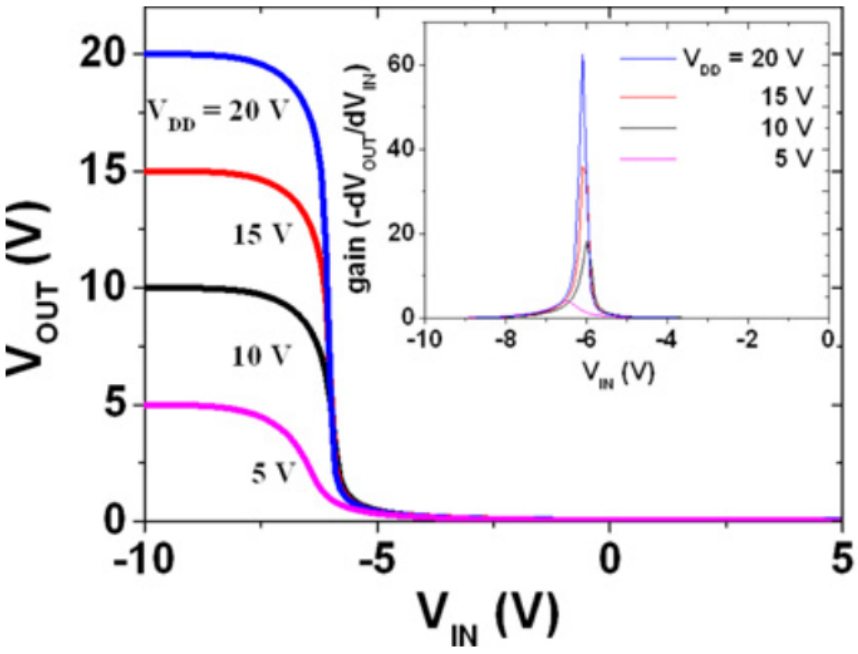

Figure 3-7. Electrical characteristics of depletion load type inverters on the flexible thin glass substrate for R∞. Insets are gains which were calculated by dV_{out}/dV_{IN} and is plotted as a function of V_{IN}.

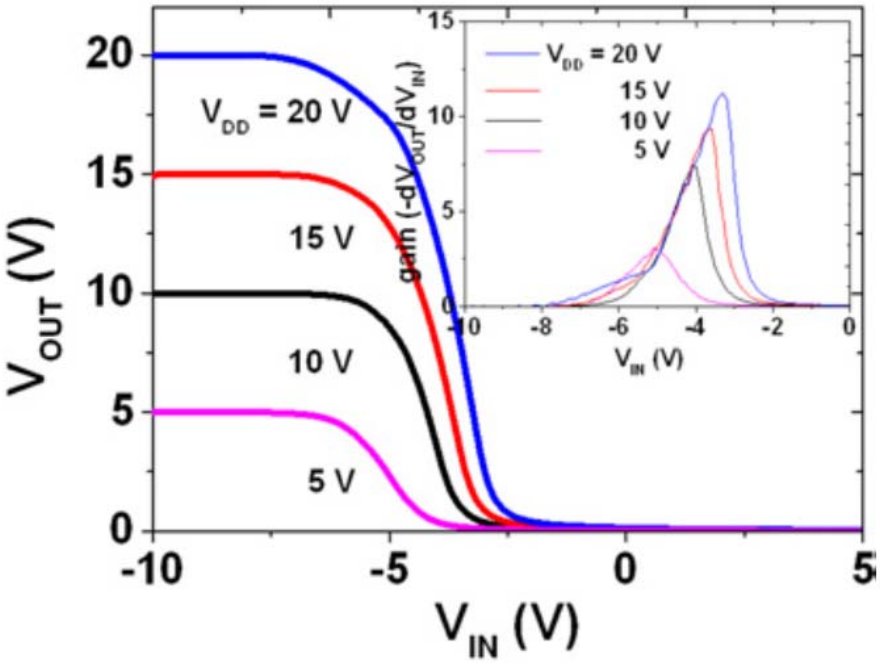

Figure 3-8. Electrical characteristics of enhancement load type inverters on the flexible thin glass substrate for R∞. Insets are gains which were calculated by dV_{out}/dV_{IN} and is plotted as a function of V_{IN}.

Figures 3-7 and 3-8 show electrical characteristics of depletion and enhancement load type inverters, respectively. W/L values of load and drive TFTs were 5/5 and 250/5 μm/μm, respectively. We used S type TFTs for measurement of inverter circuits. The inverters were operated in typical operation voltage range where V_{DD} = 5 to 20 V and V_{IN}=−10 to 5 V. The depletion type inverter shows superior performance with a high differential gain. The maximum differential gain of depletion and enhancement type inverters were $63VV^{-1}$ and $11VV^{-1}$ at V_{DD}=20V, respectively.

Since the V_{TH} values of the load and driving TFTs were negative, transition points between high to low states were in negative value of V_{IN} for both types of inverters due to the deple-

tion mode operation of the load and driving TFTs. Based on our result, it should be noted that the high performance circuits with short-channel-length transistors can be fabricated on the flexible thin glass substrate.

3.6 Prolonged positive and negative gate bias stress tests

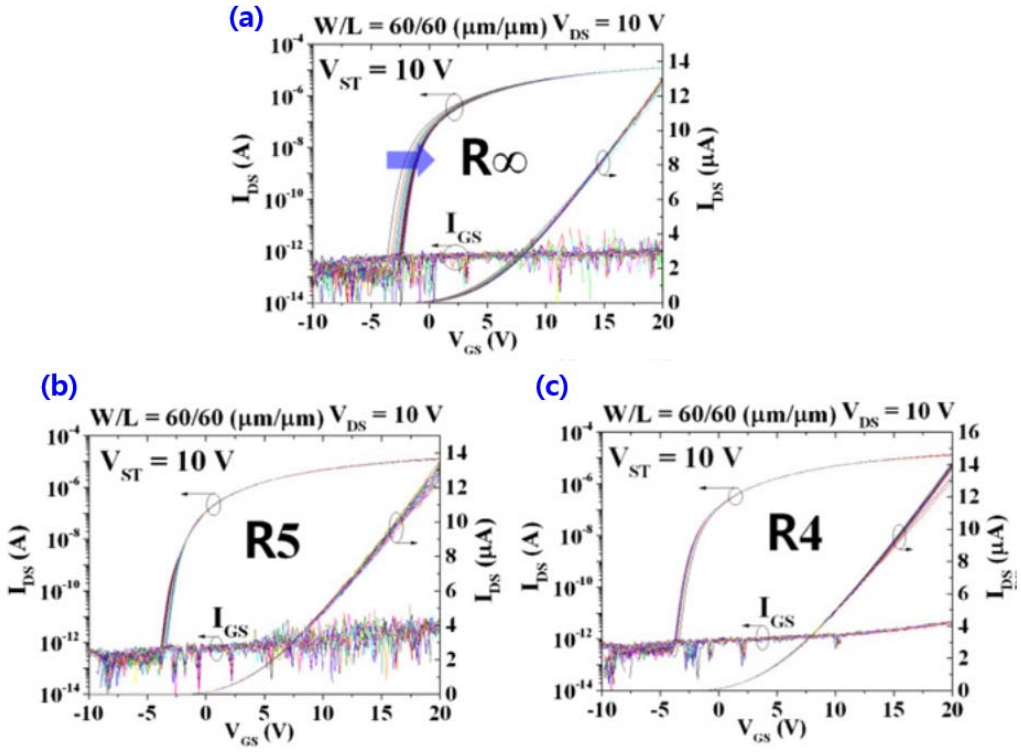

Figure 3-9. Evolutions of transfer characteristics for different bias and bending strain conditions (a) V_{ST} = 10 V, R0 (b) V_{ST} = 10 V, R5 (c) V_{ST} = 10 V, R4.

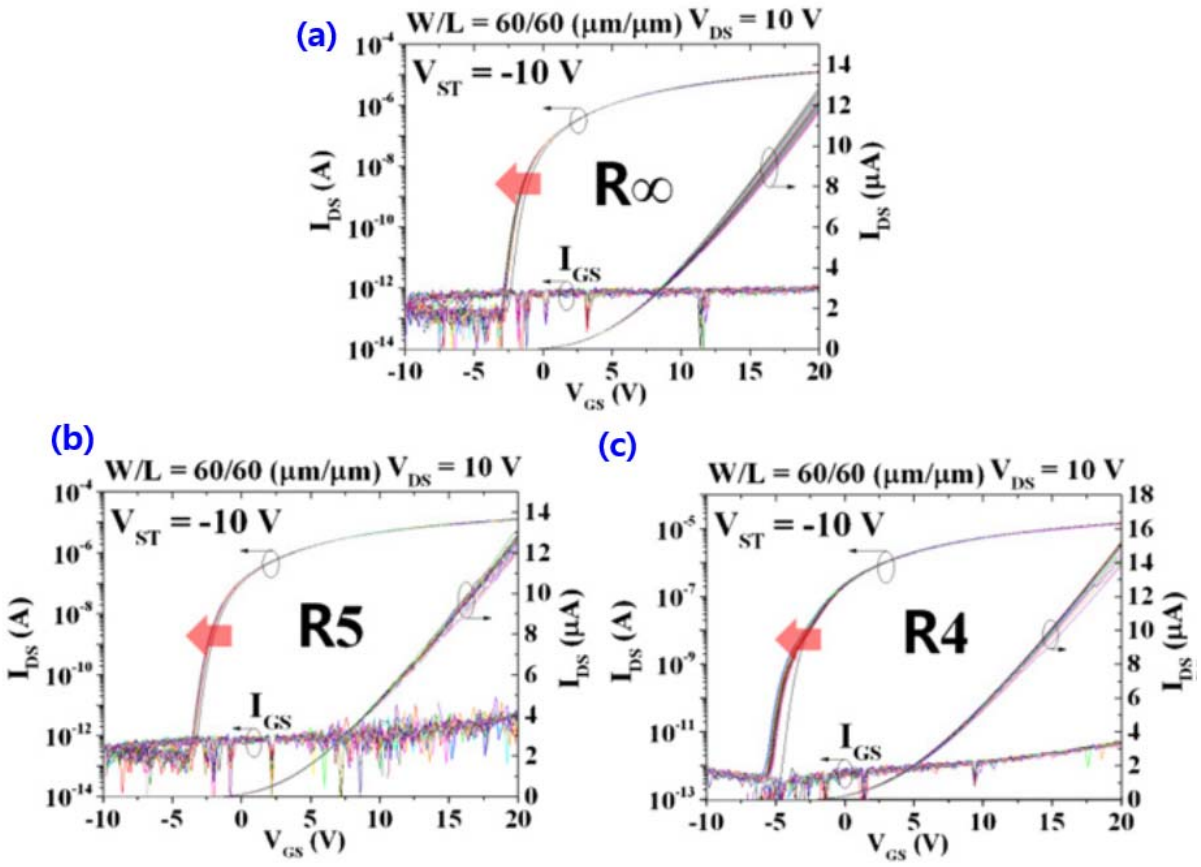

Figure 3-10. Evolutions of transfer characteristics for different bias and bending strain conditions (a) V_{ST}=−10 V, R0 (b) V_{ST}=−10 V, R5, (c) V_{ST}=−10 V, R4.

The AS sample was subjected to prolonged positive and negative gate bias stress tests for 1800 s. Figures 3-9 and 3-10 show the evolutions of transfer curve under the positive and negative gate bias stress, respectively (V_{ST} = 10 V and V_{ST} = −10 V, V_{DS} = 0 V), applying external bending strain concurrently (R∞, R5 and R4).

It is well known that if the annealing temperature is low, stability of the a-IGZO TFTs becomes poor for both positive and negative bias stress depending on the process conditions such as oxygen partial pressure.

In our case, the a-IGZO TFTs on the thin glass substrate showed positive and negative shifts

of V_{TH} under positive and negative bias stress conditions, respectively, as shown in figures 3-9 and 3-10, which is consistent with former results of instability tests of high- temperature processed a-IGZO TFTs. In particular, our a-IGZO TFTs showed very stable operation under prolonged positive and negative gate bias stress tests without a passivation layer, even when the strain is applied. The $R\infty$ sample shows somewhat larger shift of V_{TH} in comparison with those of the R5 and R4 samples when the positive bias stress is applied, which is possibly due to process variation. However, it should be noted that the variation of V_{TH} is negligible for both positive and negative bias stress conditions as shown in figures 3-9 and 3-10. In fact, when the external strain is applied, micro-cracks can be generated in the channel and channel/insulator interface regions. These micro-cracks can act as electron or hole trap sites which reduce the performance and instability of TFTs. However, the resulting bias stress instability tests of the a-IGZO TFTs reveal that the bending strain inducing micro-cracks do not influence the bias stress instability when the bending radius is larger than 40 mm and the strain is under 0.1% for both positive and negative bias stress conditions. Therefore, mechanically and electrically stable a-IGZO TFTs can be fabricated on the thin glass substrate for small bending strain conditions.

In conclusion, we demonstrated high performance, highly transparent and flexible a-IGZO TFTs and inverter circuits on a thin glass substrate. From the bending tests on the TFTs, V_{TH} was negatively shifted as an increase of the bending strain for the symmetric gate overlap sample, while the TFTs showed relatively stable operation against mechanical strain for the asymmetric gate overlap sample. Owing to the high temperature thermal annealing process,

the a-IGZO TFTs showed very good bias stress stability under prolonged positive and negative stress test. Therefore, transparent, flexible, and stable TFTs can be realized using the a-IGZO TFTs on the thin glass substrate which can open a new topic for flexible display applications.

IV. STRUCTURAL EFFECT OF HOLE WITH ELECTRODE AND a-InGaZnO THIN FILM TRANSISTOR

4.1 Introduction

Recently, bendable thin-film transistors (TFTs) have been intensively studied as switching and driving devices for application to flexible electronics. In particular, amorphous indium gallium zinc oxide (a-IGZO) TFTs was considered as one of immense attracted switching component owing to their high optical and electrical characteristics than conventional hydrogenated amorphous silicon (a-Si:H) TFTs.

In particular, to meet the requirements of transparency and flexibility at the same, a-IGZO TFTs are considered as a good candidate for switching or driving devices. Several groups have reported the electrical characteristics of transparent a-IGZO TFTs on plastic substrates, such as polyethylene naphthalate (PEN) and polyethylene terephthalate (PET) for flexible or rollable display applications using a low-temperature process. However, the low-temperature process for an a-IGZO active layer decreases the performance of the a-IGZO TFT including field-effect mobility and bias stress stability, which reduce the merits of oxide-based TFTs. For high-temperature annealing process, polyimide (PI) substrates are frequently used for fabrication of the a-IGZO TFTs, which cannot be applied to transparent display applications due to the inherent yellowish color of the PI substrates. In addition, to achieve high transparency, high performance and good bias stress stability, a high-temperature thermal annealing

process on a transparent substrate is essential during the fabrication process. Meanwhile, leading display companies have begun research for curved organic light-emitting diode television which can increase the visibility from various viewing positions. Though the minimum bending radius of these types of display is relatively large in comparison with that of conventional flexible or stretchable devices, it can be expected that slight decreases in the bending radius using thin glass greatly increases the visibility of the display. Most of the research on the bendable a-IGZO TFTs has focus on standard structure of TFTs such like planar and vertical types on flexible plastic substrates. In this case, TFTs was easily occurred electrical failure by micro-cracks in conditions of prolonged mechanical bending strain. In this study, we propose a-IGZO TFTs with hole-array structure to improve their electrical and mechanical characteristics in unfavorable bending conditions.

4.2 Device Structure and Fabrication

An IGZO TFT with hole-array structure was fabricated on manufactured 125 um-thick polyimide film. First, a 100 nm-thick Cr was deposited and patterned by using DC magnetron sputtering system and conventional photolithography as gate metal. Next, 200nm-thick SiO_2 insulator layer was deposited using PECVD at 350°C. Then, 80 nm-thick a-IGZO channel layer was sputtered and patterned by a wet etching process. To enhance the a-IGZO TFT performance and device stability, thermal annealing process was performed in an air ambient at 300 °C for 1 h. Subsequently, gate via was formed by a photolithography and a reactive ion

etching (RIE) method. Next, a 100 nm-thick Al layer was deposited and patterned by evaporator and a lift-off process. Finally, the hole-array structure was formed on channel and source/drain region by using dry etching method.

4.3 The Hole Drilling Method

The hole drilling method is a method for measuring residual stresses in a material. Residual stress occurs in a material in the absence of external loads. Residual stress interacts with the applied loading on the material to affect the overall strength, fatigue, and corrosion performance of the material. Residual stresses are measured through experiments. The hole drilling method is one of the most used methods for residual stress measurement.

The hole drilling method can measure macroscopic residual stresses near the material surface. The principle is based on drilling of a small hole into the material. When the material containing residual stress is removed the remaining material reaches a new equilibrium state. The new equilibrium state has associated deformations around the drilled hole. The deformations are related to the residual stress in the volume of material that was removed through drilling. The deformations around the hole are measured during the experiment using strain gauges or optical methods. The original residual stress in the material is calculated from the measured deformations. The hole drilling method is popular for its simplicity and it is suitable for a wide range of applications and materials.

Key advantages of the hole drilling method include rapid preparation, versatility of the tech-

nique for different materials, and reliability. Conversely, the hole drilling method is limited in depth of analysis, specimen geometry, and at least semi-destructive.

Kirsch's solution for stresses at a hole are for the case of uniaxial tension in an infinite plate. Uniaxial tension is represented by the remote stress, σ_∞. The hole has radius, a, the radial coordinate is r (which is meaningless when r<a), and $\theta = 0$ aligns with the remote loading direction. We will see that the famous factor-of-three stress concentration occurs at $\theta = \pm 90^\circ$.

$$\sigma_{rr} = \frac{\sigma_\infty}{2}\left(1 - \left(\frac{a}{r}\right)^2\right) + \frac{\sigma_\infty}{2}\left(1 - 4\left(\frac{a}{r}\right)^2 + 3\left(\frac{a}{r}\right)^4\right)\cos 2\theta$$

$$\sigma_{\theta\theta} = \frac{\sigma_\infty}{2}\left(1 + \left(\frac{a}{r}\right)^2\right) - \frac{\sigma_\infty}{2}\left(1 + 3\left(\frac{a}{r}\right)^4\right)\cos 2\theta$$

$$\tau_{r\theta} = -\frac{\sigma_\infty}{2}\left(1 + 2\left(\frac{a}{r}\right)^2 - 3\left(\frac{a}{r}\right)^4\right)\sin 2\theta$$

At Infinity

At $r = \infty$, all the a/r terms go to zero, leaving

$$\sigma_{rr} = \frac{\sigma_\infty}{2} + \frac{\sigma_\infty}{2}\cos 2\theta$$

$$\sigma_{\theta\theta} = \frac{\sigma_\infty}{2} - \frac{\sigma_\infty}{2}\cos 2\theta$$

$$\tau_{r\theta} = -\frac{\sigma_\infty}{2}\sin 2\theta$$

and $\sigma_{rr} = \sigma_\infty$ when $\theta = 0^\circ$ and 180°, while $\sigma_{\theta\theta} = \sigma_\infty$ when $\theta = \pm 90^\circ$, as they must be. The shear stress, $\tau_{r\theta}$, is simply the result of coordinate transformations on σ_∞.

At The Hole

At r=a, all the a/r terms equal one, producing

$$\sigma_{rr} = 0$$

$$\sigma_{\theta\theta} = \sigma_{\infty}(1 - 2\cos 2\theta)$$

$$\tau_{r\theta} = 0$$

The radial stress, σ_{rr}, and the shear stress, $\tau_{r\theta}$, are zero at the hole because it is a free surface. It is the hoop stress, $\sigma_{\theta\theta}$, that merits attention. At $\theta=0$, $\sigma_{\theta\theta}=-\sigma_{\infty}$, so the hoop stress is actually compressive. However, it is at $\theta=\pm 90^{\circ}$ that $\sigma_{\theta\theta}=3\sigma_{\infty}$ and the factor-of-three stress ratio occurs. This ratio is called the Stress Concentration Factor and is discussed below.

This is the largest stress at the hole, and therefore the first value to compare to a material's yield strength to check for yielding. The stress state is uniaxial, so the $\sigma_{\theta\theta}$ value is also the effective or von Mises stress that can be directly compared to the material's yeild strength.

4.4 Various hole-array structure

First of all, to solve the damage of interconnect, we attempt structurally change the electrode as use several types hole structure, such as square and triangular hole-array structure in figure 4-1. These structure reduced the strain by tensile or compression force. The hole drilling method can measure microscopic residual stresses near the material surface. Base on this principle, hole-array structure was achieved from ANSYS simulator in figure 4-2.

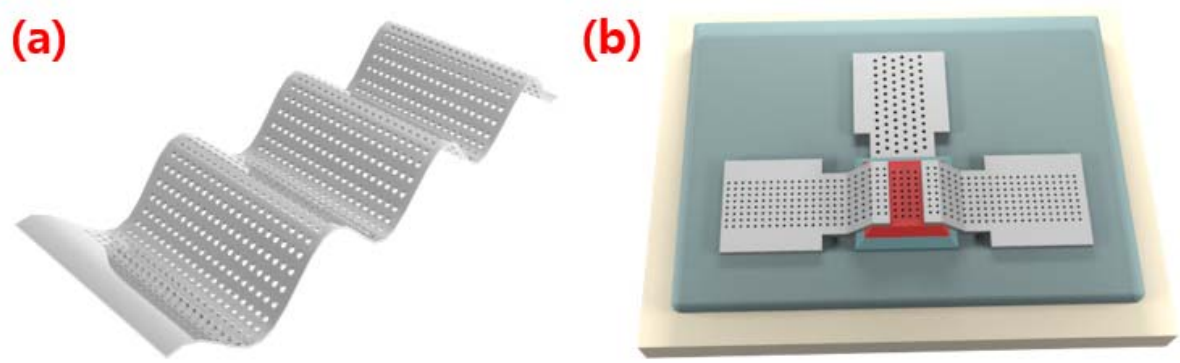

Figure 4-1. A schematic diagrams of (a) electrode and (b) TFT.

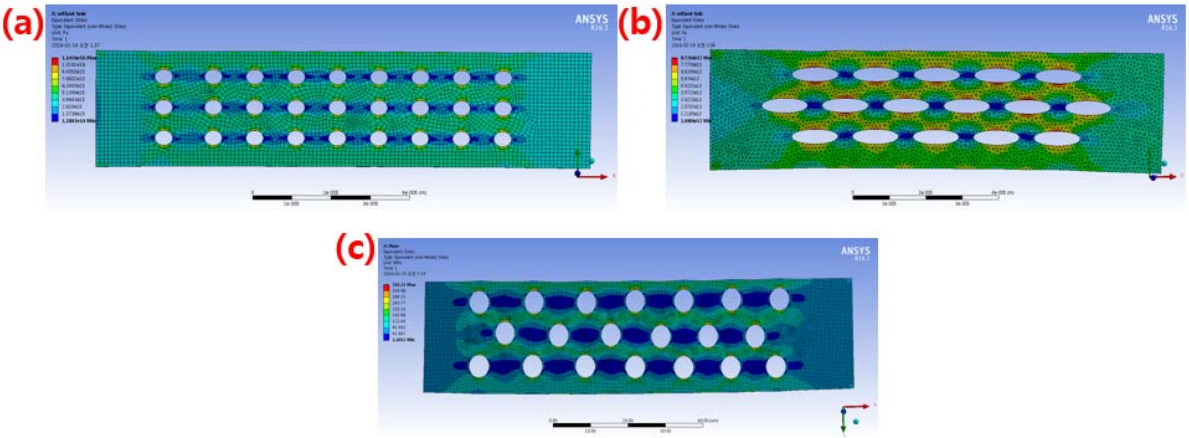

Figure 4-2 Simulated results of electrode with various hole-array structure.

Increasing the hole diameter or decreasing the plate width in a finite width plate will increase the maximum stress at the hole.

Figure 4-3 is aluminum electrode without hole structure. In this study, aluminum film was used source drain electrode. Al has originally high ductility as you can see the material ductility table. After bending, Al was shown wrinkled surface.

Two kinds of electrodes were fabricated and tested on polyimide film. Aluminum and IZO

film is used in this experiment. The electrode has diameter hole from 2um to 5 um, with triangular and square array structure in figure 4-3.

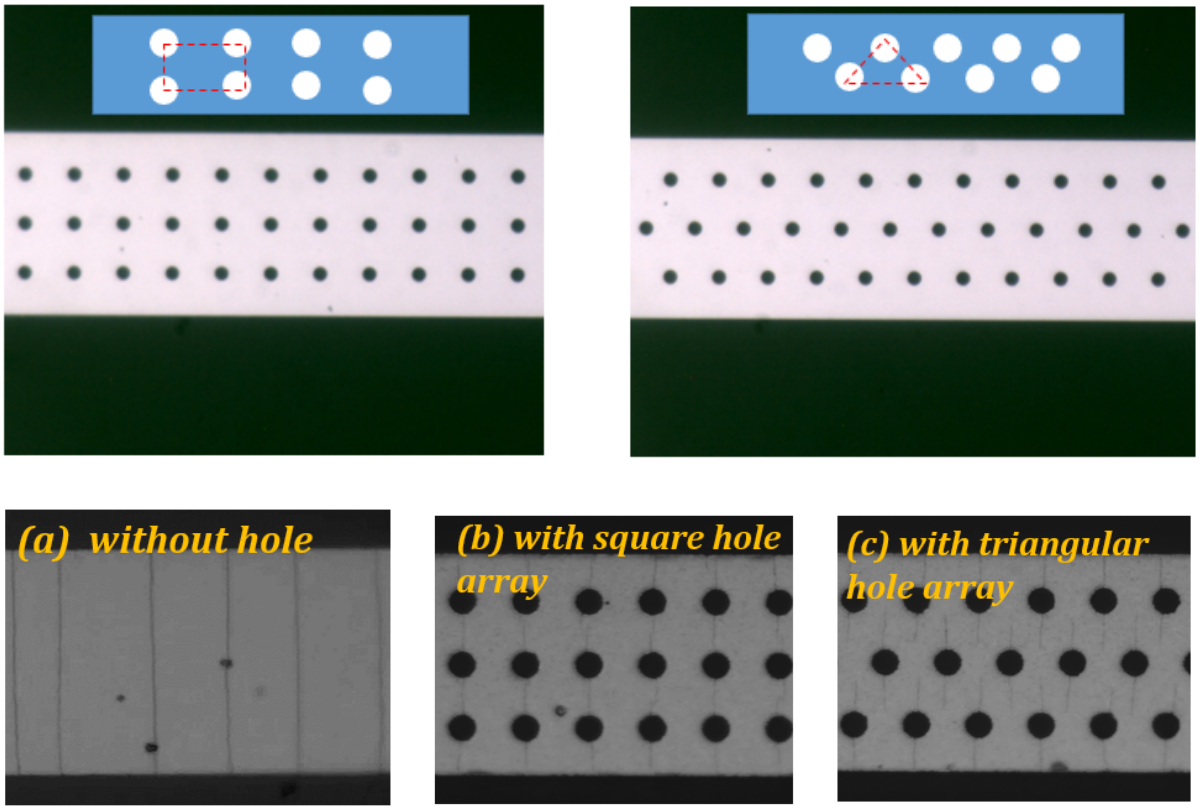

Figure 4-3. SEM images of electrode without hole and with hole array structure after bending

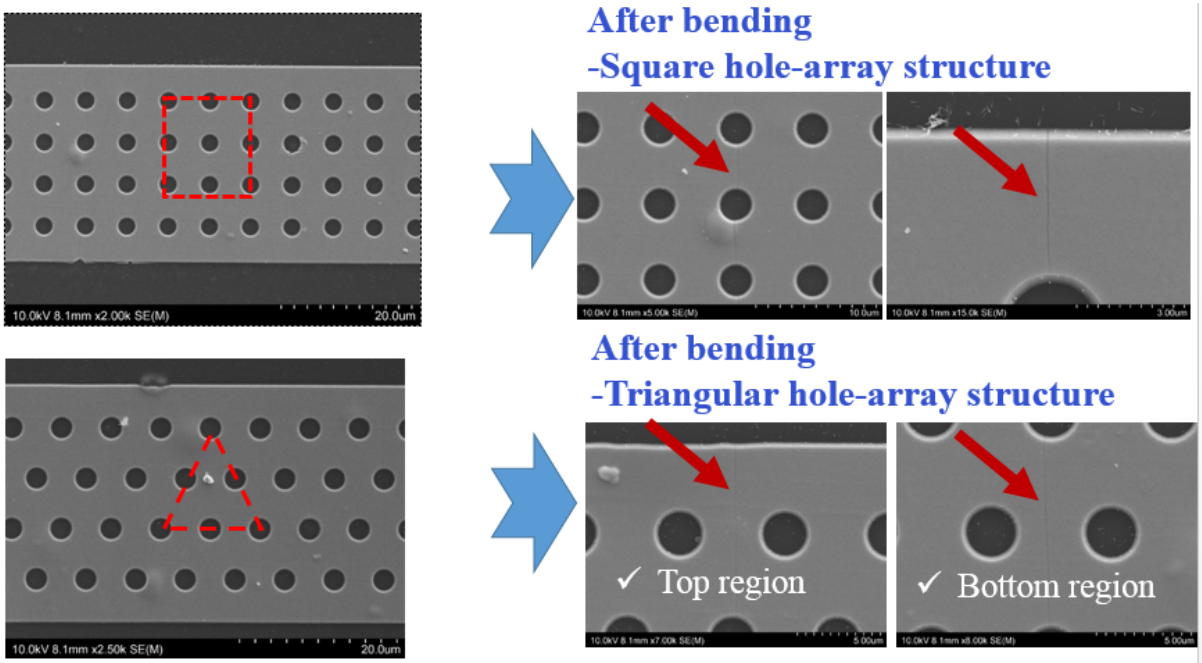

Figure 4-4. Oxide thin film with triangular and square hole-array structure.

In square hole-array structure, crack was easily generated between each hole. At near the hole, crack was completely generated.

After that, we try to the bending test as using this electrode and proved the effect of stress relief hole and stop hole in thin film. The hole-array has a good effect for improvement of fatigue resistance. The resistance of all electrode lines were increased by the bending cycle.

The good efficiency in bending state is small sized hole as you can see the graph. Triangular hole-array structure is robust than the square hole-array structure.

In square hole-array structure, cracks was completely generated in top to bottom. But in triangular hole-array structure crack was stopped between the each holes in figure 4-4. In bending state, originally oxide film was easily cracked. But the hole-array structure reduce the fatigue resistance in oxide film.

The oxide film with triangular hole-array structure was also better robust than the square hole-array structure. In the triangular hole-array structure, the crack was stopped between each holes. Base on the experiments of electrode with hole-array structure. We fabricated strain reduced robust a-IGZO TFT with hole array on flexible polyimide substrate.

4.5 Hole-array effect with a-IGZO active

In advance, we try to hole-array effect test for active region of a-IGZO TFT, we extracted parameter from IV curve in TFT with hole, and without hole in figure 4-5.

We obtain the similar electrical properties. But in source drain current of TFT with hole was depressed compare to TFT without hole. The reason results from reduced active area in TFT.

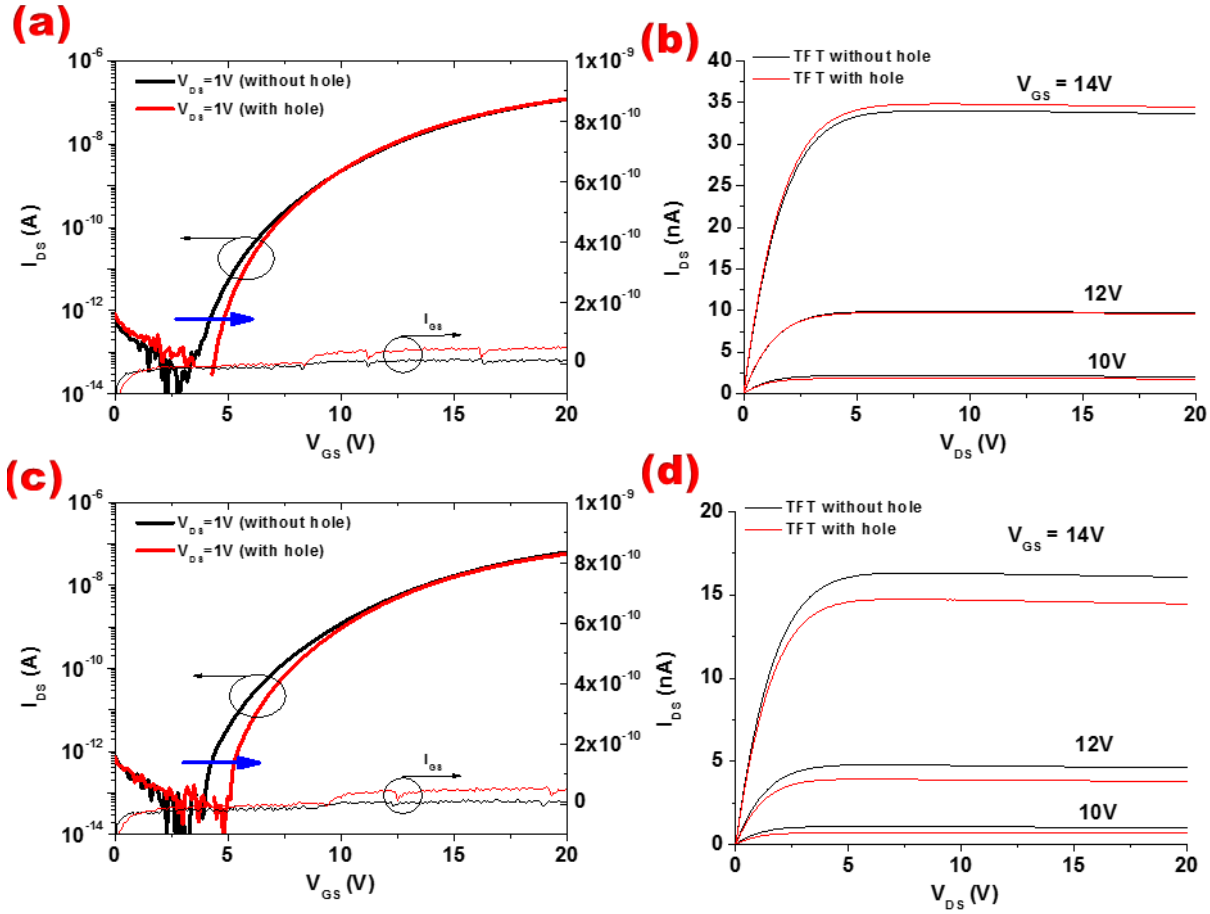

Figure 4-5. Evolutions of transfer characteristics for TFT without hole-array and with hole-array on heavily doped Si substrate.

Finally, we try to the bending test using this samples. The electrical characteristics were slightly changed in subthreshold slope and threshold voltage.

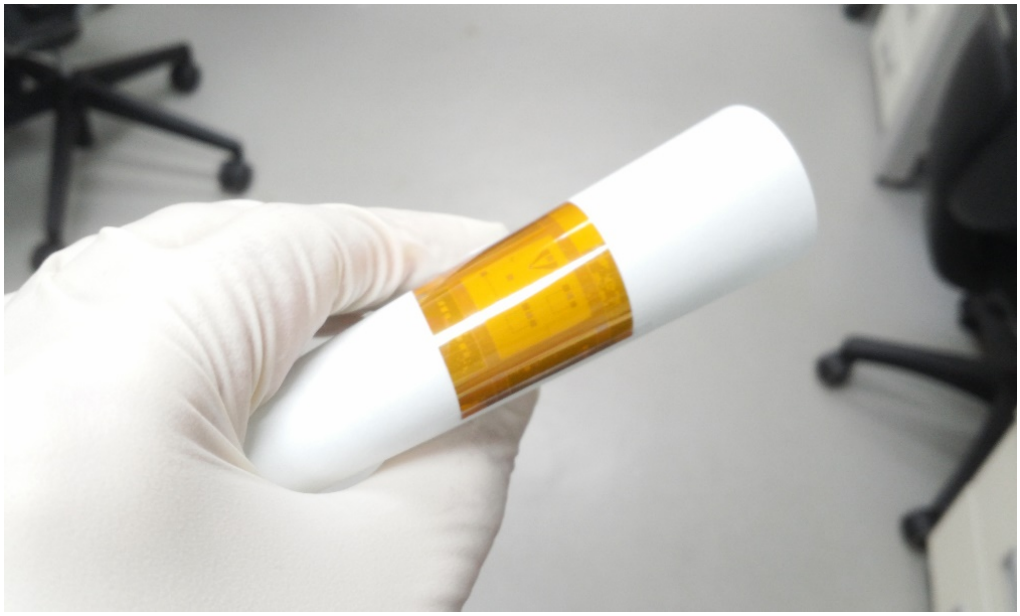

Figure 4-6. Fabricated a-IGZO TFT on polyimide film.

Figure 4-7. Folding images of a-IGZO TFT polyimide film.

The top view image of flexible a-IGZO TFT with hole-array is shown in Figure.5-8 (a) by using scanning electron microscope (SEM) system. Two types of a-IGZO TFTs were fabri-

cated, which have with and without hole-array structure. Figure 4-8 (b) shows the transfer characteristics with and without hole of a-IGZO TFTs as function of hole diameter. The device performance shows a high field effect mobility of > 6 $cm^2/V \cdot s$, a subthreshold slope of > 700 mV/decade, drain current on-off ratio of > 10^6 in both types of a-IGZO TFTs. The bending test of a-IGZO TFTs on the polyimide substrate was performed using semicircular shaped curvature. The bending radius was set to 100 mm by considering minimum bending radius (tensile strain of 0.22 % perpendicular to the channel current flow). The a-IGZO TFTs with hole-array remarkably reduced electrical failure caused by micro-cracks induced mechanical strain than TFT without hole-array samples.

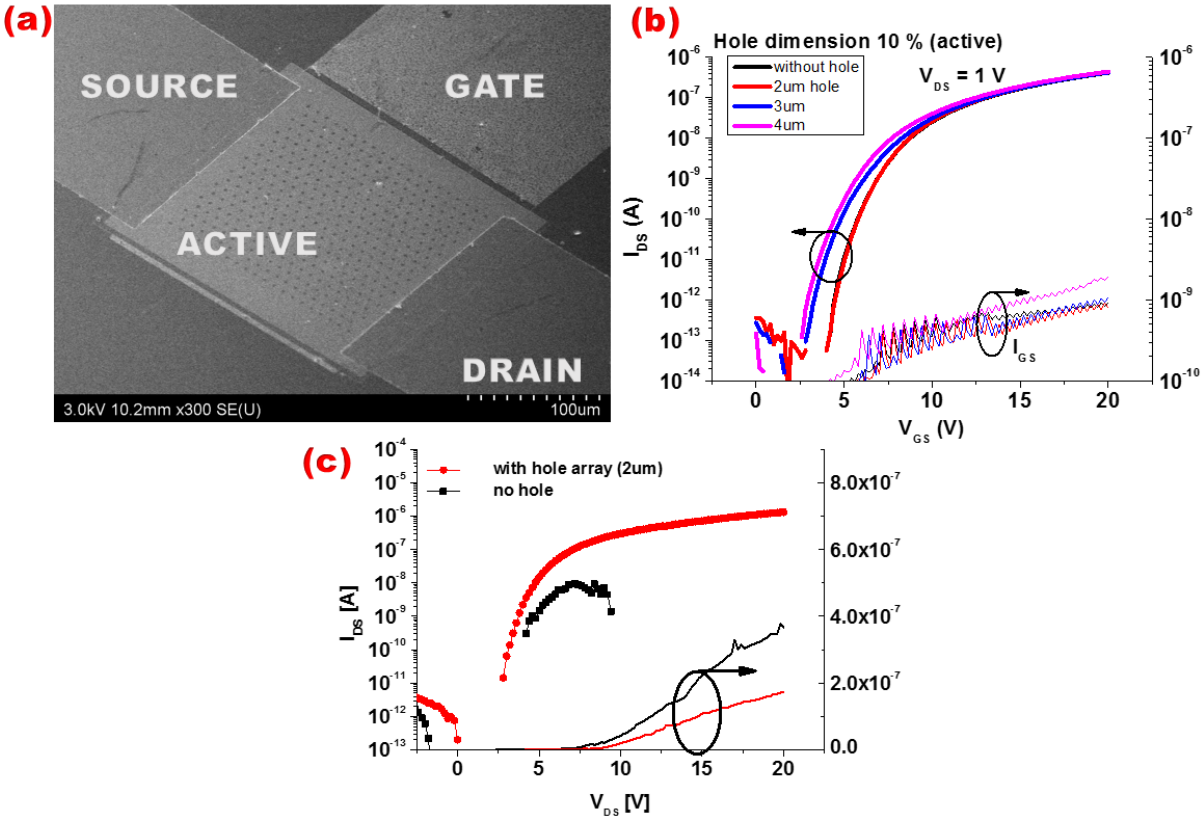

Figure 4-8. Evolutions of transfer characteristics for TFT without hole-array and with hole-array after bending.

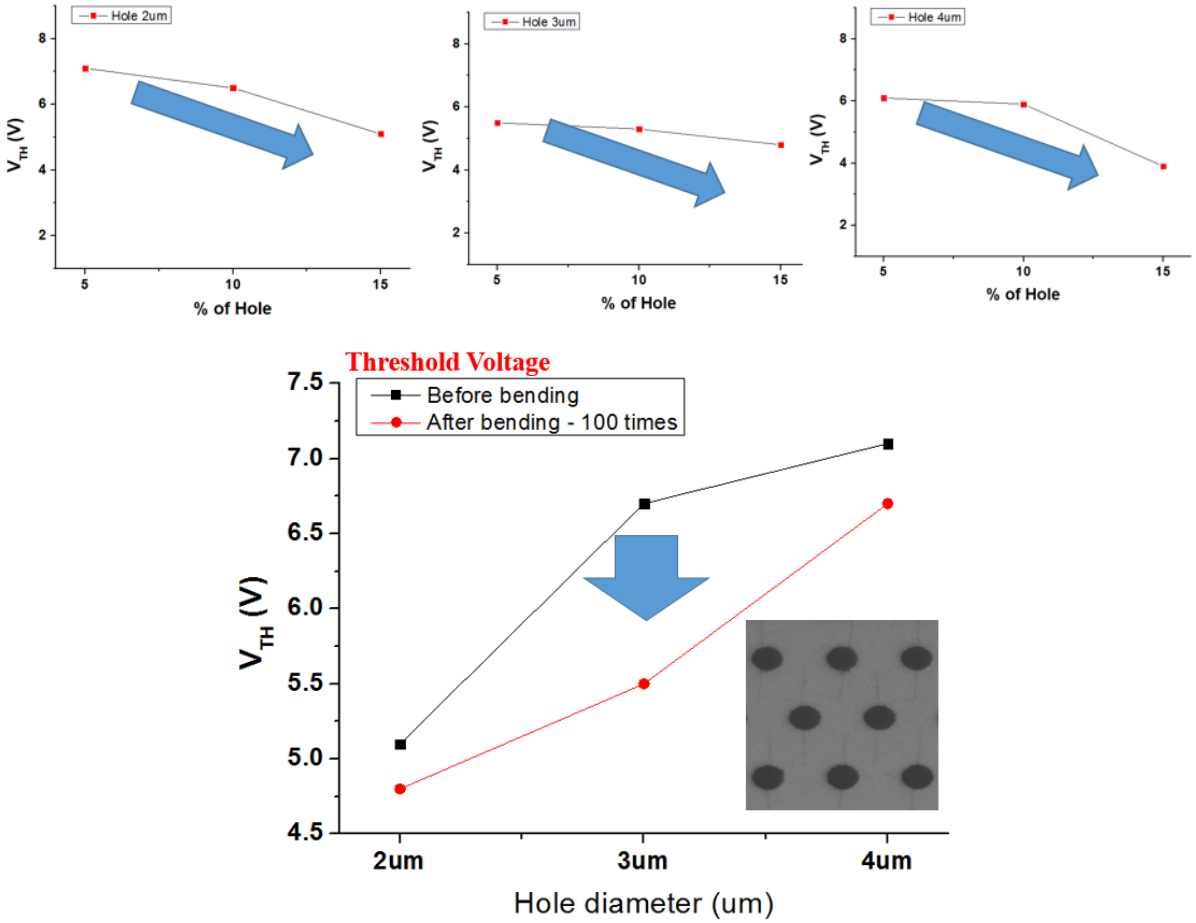

Figure 4-9. Electrical changes of a-IGZO TFT after 100 times folding

In conclusion, we demonstrated high performance and flexible a-IGZO TFTs with hole-array on polyimide substrate and investigated the variation in the electrical characteristics as a function of hole area and radius. The a-IGZO TFTs with hole-array device performance shows good electrical characteristics and the mechanical strain reduced remarkably in hole-array structure as compared with the TFT without hole-array. Thus, hole-array structure of a-IGZO TFTs can give an important merit to use flexible devices.

V. CONCLUSION

The research has been to study the novel oxide based TFTs on a flexible platform. Amorphous Indium Gallium Zinc Oxide was based since among the different flavors of metal oxide thin films actively pursued in recent years, a-IGZO has obtained considerable interest based on device performance and reproducibility using commercially feasible, large area processing techniques. Thin glass and polyimide film was the substrate of choice since it offered dimensionally very stable flexible platform for device fabrication and it allowed greater freedom to design small features for demonstration of high performance.

One of the key features of a-IGZO TFTs have a much higher field-effect mobility (μ_{FE} = >10 $cm^2/V \cdot s$) compared to a-Si:H TFTs, a low threshold voltage exhibiting in enhancement mode operation, excellent switching properties, and a small parasitic series resistance employing IZO as source/drain electrode without the additional contact doping process. Process optimization of a-IGZO TFT was performed in scaling channel length, temperature-dependence and oxygen dispersion on active surface.

The scaling behaviour of a-IGZO TFTs were analysed with a-IZO transparent S/D electrodes. A decrease in field-effect mobility in the saturation region as compared with that in the linear region was found to have originated from sputtering damage that occurred during the a-IZO S/D electrodes deposition process. This becomes more prominent when the channel length is short. This also induced large parasitic resistance and a long gate overlap distance due to the long current transfer length, indicating that control of the parasitic resistance is essential for

the scaling down of a-IGZO TFTs with transparent a-IZO S/D electrodes.

A bendable a-IGZO TFTs and inverter circuits was demonstrated on a thin glass substrate. From the bending tests on the TFTs, V_{TH} was negatively shifted as an increase of the bending strain for the symmetric gate overlap sample, while the TFTs showed relatively stable operation against mechanical strain for the asymmetric gate overlap sample. Owing to the high temperature thermal annealing process, the a-IGZO TFTs showed very good bias stress stability under prolonged positive and negative stress test. Therefore, transparent, flexible, and stable TFTs can be realized using the a-IGZO TFTs on the thin glass substrate which can open a new topic for flexible display applications.

Finally, we achieved high performance and flexible a-IGZO TFTs with hole-array on polyimide substrate and investigated the variation in the electrical characteristics as a function of hole area and radius. The a-IGZO TFTs with hole-array device performance shows good electrical characteristics and the mechanical strain reduced remarkably in hole-array structure as compared with the TFT without hole-array. Electrical stability measurements of the flexible devices with a hole structure under tensile and compressive mechanical strain showed no appreciable change in the I-V characteristics during bending. The electrical characteristics under mechanical bending suggest that carrier transport was unaffected during mechanical strain. Testing under dc gate bias conditions, the electrical stability of the TFTs showed a positive VT shift of 3.8 V after 3600 s without any change in subthreshold-swing (S.S.). The a-IGZO TFTs with hole array structure exhibits high on/off ratio of >106 and field effect mobility of >6 $cm^2/V \cdot s$ even after high bending radius. The bending radius was set to 100 mm

by considering minimum bending radius (tensile strain of 0.22 % perpendicular to the channel current flow). The a-IGZO TFTs with hole-array remarkably reduced more electrical failure than TFT without hole-array samples since disconnected micro-cracks induced the release of mechanical strain. Thus, proposed hole-array structure of a-IGZO TFTs can give an important merit to use flexible devices.

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요 약 문

유연소자 응용을 위한 비정질 InGaZnO 박막트랜지스터의 공정 및 전기적 특성분석

디스플레이 시장의 차세대 기술로 평가되는 유연 디스플레이는 평면 디스플레이와는 달리 접거나 휠 수 있는 등 형태를 변형시킬 수 있는 디스플레이 기술로서, 패시브 및 액티브 소자로 구성된 회로 소자를 플라스틱 등 휠 수 있는 기판에 제작되어, 디스플레이로서는 우수한 표시특성을 가지면서 구부리거나 접히는 조건에서도 기계적, 전기적인 신뢰성을 가지는 기술 분야이다. 최근 유연 디스플레이 기술분야 중 액티브 소자로 유연 기판에 사용되는 반도체 물질로 비정질 산화물 반도체가 각광을 받고 있다. 그 가운데서도, 비정질 InGaZnO 박막이 트랜지스터의 반도체 부분으로 가장 많은 연구가 진행되고 있는데, 이는 비정질인 특성과 상온 증착이 가능하여 대면적 균일도 및 공정상의 이점이 크며, 전자이동도가 비정질임에도 불구하고 10cm^2/Vs 가 넘는 우수한 전기적 특성을 보이고 있으며, 3.2 eV 정도의 밴드갭을 가짐으로써 가시광 영역에서 높은 투과율로 인하여 투명 디스플레이로서의 활용도 가능한 이점을 가지고 있다.

근래에는 비정질 InGaZnO 박막을 활용하여 유연 디스플레이의 액티브 소자로 다양한 연구가 진행되고 있으나, 구부리거나 접힌 상태에서의 물리적 전기적 특성에 대한 연구는 아직까지는 초보적인 수준이 이르고 있다. 따라서 유연 소자로의 응용을 위해서는 구부리거나 접히는 유연 상태에서의 물리적 전기적 특성에 대한 연구가 반드시 필요하다고 볼 수 있다.

본 연구에서는 유연성 디스플레이에 적용할 수 있는 견고한 비정질 InGaZnO 박막트랜지스터를 제작하기 위해 다양한 기판에서의 비정질 InGaZnO 박막트랜지스터를 공정하여 그 전기적, 기계적 특성을 분석하였다. 첫째로 비절질 InGaZnO 박막트랜지스터의 채널 길이별 특성을 분석하기 위해 두 가지 종류의 소자를 제작하였다. 먼저 고농도로 도핑된 Si 기판을 back gate 로 이용하여, 미세패턴 형성 기술로 제작한 비정질 IGZO TFT 의 성능을 향상시키기 위해 채널 길이, 온도 및 대기 중 기체 반응에 의한 비정질 IGZO TFT 의 전기적 최적화 조건을 확인하였다. 이러한 분석을 기반으로 유연한 유리기판으로부터 플라스틱기판에 이르기까지 유연한 소자를 제작하였고, 소자의 제작은 인버터 등의 기본소자 제작을 통한 회로의 기본 구성요소로서의 특성을 평가하였다. 비정질 IGZO 박막트랜지스터의 기본적인 특성을 바탕으로 최근 이슈가 되고 있는 커브드 디스플레이에서의 응용을 위해 매우 얇은 유리기판 위에

비정질 IGZO 박막트랜지스터 소자를 제작하여, 강한 구부림 가운데서 문턱전압의 낮은 변화율 및 장시간의 바이어스 스트레스에도 전기적 특성에 변화가 없는 박막트랜지스터의 결과를 얻었으며, 또한 폴리이미드 유연기판을 활용하여 비정질 InGaZnO 박막트랜지스터에서의 마이크로 홀의 구조적 변형을 통한 전기적 특성을 파악하였다. 다양한 형태의 홀 구조에서 균열현상을 파악하고, 이는 ANSYS 를 이용하여 그 원리를 시뮬레이션 하였다. 최적화된 삼각형 배열의 홀 구조를 활용하여 첫째로 전극에 적용하여 구부림 정도에 따른 균열현상을 파악하였으며, 이를 바탕으로 폴리이미드를 기판으로 하는 비정질 InGaZnO 박막트랜지스터에 적용하여 전기적 특성을 추출하였다. 이러한 홀 형태의 구조는 강한 구부림에서 매우 견고한 특성과 우수한 전기적인 특성을 보였으며, 이는 유연성 디스플레이를 기반으로 하는 다양한 메탈전극 및 반도체에 적극 활용할 수 있을 것으로 사료된다.

핵심어: a-IGZO 박막트랜지스터, 유연성 전자소자, 홀구조, 플렉서블 디바이스