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Quantitative Analysis on the Interaction Between Channel Carrier and Remote Trap in $Hf_xZr_{1-x}O_2/SiO_2$ Interface in Ferroelectric Field-Effect-Transistor

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ABSTRACT

In this work, the polarization-dependent operating characteristics of TiN/$Hf_xZr_{1-x}O_2$(HZO)/SiO_2/Si ferroelectric FETs (FeFETs) are investigated, and remote HZO/SiO_2 interface traps ($D_{it,FE/DE}$) are quantitatively separated from Si/SiO_2 interface traps (D_{it0}). X-ray photoelectron spectroscopy (XPS) reveals an oxygen-vacancy (V_O)-rich $HfSiO_x$ layer at the HZO/SiO_2 interface. Based on the transistor operation theory and trap/polarization-switching charge distribution, the difference in the W1 and W0 states is determined by whether the HZO/SiO_2 interface traps are filled and emptied, respectively. Subthreshold current method (SCM) shows that *SS* increases from ~95 mV/dec (W1 state) to 110 mV/dec (W0 state), yielding effective interface trap density ($D_{it,eff}$) values of 4×10^{12} and 7.8×10^{12} $cm^{-2}eV^{-1}$, respectively; their difference (3.8×10^{12} $cm^{-2}eV^{-1}$) corresponds to $D_{it,FE/DE}$. Methods that exploit the frequency-dependent response of the defect states–Multi-frequency C-V (MFCV) and Terman method (TM)–yield D_{it0} and $D_{it,FE/DE}$ values that match the SCM results. Accounting for the capacitive-projection factor of 2.5, the actual HZO/SiO_2 interface trap density ($D_{FE/DE}$) is ~1×10^{13} $cm^{-2}eV^{-1}$, approximately 2.5 times higher than D_{it0}. The combined SCM-MFCV-TM framework thus furnishes a rapid, purely electrical metric for monitoring HZO/SiO_2 quality and guides strategies to suppress remote trap-carrier interaction (RTCI)-driven degradation in FeFET performance.

1 | Introduction

The relentless demand for fast, energy-efficient, and densely integrated non-volatile memory (NVM) has stimulated intense research into ferroelectric field-effect transistors (FeFETs) based on hafnium oxide (HfO_2) [1–4] Unlike conventional charge-storage flash, FeFETs store information in the remanent polarization (P_r) of an ultrathin ferroelectric layer [5–7], enabling nanosecond-order write speed, sub-3 V operation, and intrinsic compatibility with complementary metal-oxide-semiconductor (CMOS) logic [8–10]. Among the various device architectures, the metal-ferroelectric-insulator-semiconductor (MFIS) stack–typically TiN/$HfZrO_2$(HZO)/SiO_2/Si–has emerged as a front-runner for embedded NVM because it leverages the existing SiO_2 interfacial layer (IL) that is indispensable for high electron

Abbreviations: MFCV, Multifrequency C-V Method; RTCI, Remote trap-carrier interaction; SCM, Subthreshold Current Method; TM, Terman Method.

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mobility with reasonable Si/SiO_2 interface quality in advanced logic nodes [11, 12].

However, the advantages of MFIS FeFETs are presently curtailed by reliability issues that originate from charge traps at or near the ferroelectric/dielectric (FE/DE) interface. Both experimental reports and physics-based simulations agree that carrier tunneling from the semiconductor surface can populate a distribution of stored charges in traps located at the HZO/SiO_2 interface, and even with the ferroelectric and dielectric bulk [13–15]. The trapped charges generate an internal electric field that opposes polarization switching, leading to memory-window (MW) shrinkage, read-after-write latency (RWL) delay, endurance degradation, and charge trapping-assisted retention loss [16]. Because the capture and emission time constants of these traps span milliseconds to hours, they evade detection in high-frequency capacitance measurements and pulsed write operations that are commonly employed to benchmark FeFET performance [17, 18]. Conversely, quasi-static transfer characteristics (DC *I-V*) and time-dependent current relaxation experiments reveal pronounced distortions that mask the intrinsic ferroelectric behavior and complicate device optimization.

To date, quantitative de-embedding of such slow and deep trap states from the overall electrical response remains elusive, partly because most metrology has focused on the Si/SiO_2 interface where traditional MOSFET reliability models apply [19]. Yet, recent spectroscopic evidence indicates that the density of interface traps (D_{it}) at the buried HZO/SiO_2 interface can rival–or even exceed–that at Si/SiO_2, especially when defect states accumulate during the high-temperature ferroelectric crystallization anneal [20]. A quantitative analysis and robust methodology to isolate and quantify these remote defects are therefore a prerequisite for rational process optimization and reliability of MFIS FeFETs.

In this work, we first analyze the observed polarization-dependent differences in device operating characteristics. In addition, we present a comprehensive electrical-diagnostic framework that disentangles the contributions of remote slow traps at the HZO/SiO_2 interface from those of the conventional Si/SiO_2 interface traps in MFIS FeFETs. Using a combination of subthreshold current method (SCM), multi-frequency *C–V* (MFCV), and Terman method (TM), we extract the trap density and energy distribution associated with the HZO/SiO_2 interface. The proposed methodology provides a straightforward methodology to electrically monitor the interfacial quality of MFIS stacks without recourse to material perspective analysis technologies [21–26].

2 | Experimental Methods

We fabricated MFIS-structure FeFETs using a conventional 0.5 μm gate-last CMOS process on a six-inch silicon-on-insulator (SOI) wafer, as illustrated in Figure 1a. The devices were constructed on a 100 nm thick p-type silicon-on-insulator (SOI) layer, over which a SiO_2 interlayer, a HZO ferroelectric film, and a TiN top gate electrode were sequentially deposited. After patterning the TiN top gate by the reactive ion etch process, the ion implantation process for source and drain formation is performed, followed by rapid thermal annealing for crystallization of HZO film and dopant activation. Finally, the source and drain contacts open, and the metallization process is conducted to form a contact pad. The fabrication steps are illustrated in Figure S1. The cross-sectional transmission electron microscope (TEM) image in Figure 1b confirms that the structure of the fabricated device is as expected. The high-resolution magnified image shows the uniform thickness of the HZO and SiO_2 layers, approximately 6.1 and 1.2 nm, respectively, with crystallinity in the HZO film. In the same manner, the energy dispersive spectroscopy (EDS) elemental mapping in Figure 1c shows the spatial distribution of Hf, Zr, Ti, Si, O, and N within the gate stack. The homogeneous distribution of Hf and Zr across the HZO layer confirms that the insulating film is a mixed Hf-Zr oxide. The grazing-incidence x-ray diffraction (GI-XRD) result shown in Figure 1d was utilized to analyze the crystallographic phases of the HZO film. The diffraction peaks observed around $2\theta \approx 30.5°$ and 35.5° correspond to the (111) and (020) planes of the orthorhombic phases; and (011) and (002) planes of the tetragonal phases, confirming the presence of the ferroelectric o-phase in the film [27, 28]. The EDS scan result along the gate stack and GI-XRD peak analysis result are depicted in Figure S2.

Figure 1e presents the electrical characterization of the fabricated FeFETs by positive-up-negative-down (PUND) measurement. The polarization-gate voltage ($P–V_G$) hysteresis loop and the corresponding switching current (J_{SW}) curve were measured, and a well-defined hysteresis loop is evident, indicating successful polarization switching. The observed coercive voltage (V_C) was $\sim \pm 2.5$ V, considering the peaks were observed in the J_{SW} near ± 2.5 V. The measurement system and equipment are illustrated in Figure S3.

3 | Results and Discussion

3.1 | DC Transfer Curves and Subthreshold Slope Variation Depending on Polarization State

From the transfer curves measured in the fabricated FeFET, a difference in subthreshold slope (*SS*) depending on polarization state is observed (see Figure 2a,b). We investigated the physical origin of the observed variation in *SS* between the high and low V_T states–W0 and W1 states–of the same FeFET. *SS* is generally regarded as an indicator of how effectively the applied V_G modulates the surface potential of the silicon channel (ψ_s), and is fundamentally governed by the body coupling factor, $m = (d\psi_s/dV_G)^{-1}$. In conventional Si-MOSFETs, degradation of *SS* is typically attributed to the presence of interface traps, particularly those located at the Si/SiO_2 interface. These trap states screen the V_G through charge trapping, thereby reducing the efficiency with which the V_G modulates ψ_s [19, 22, 23]. This phenomenon is quantitatively described by the dependence of the *m* factor on the Si/SiO_2 interface state capacitance, C_{it}, which can be extracted from the calculated SS using the following expression:

$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) = \ln(10)\frac{mkT}{q} \quad (1)$$

where C_d is the depletion capacitance of the silicon channel, and C_{ox} is the gate insulator capacitance.

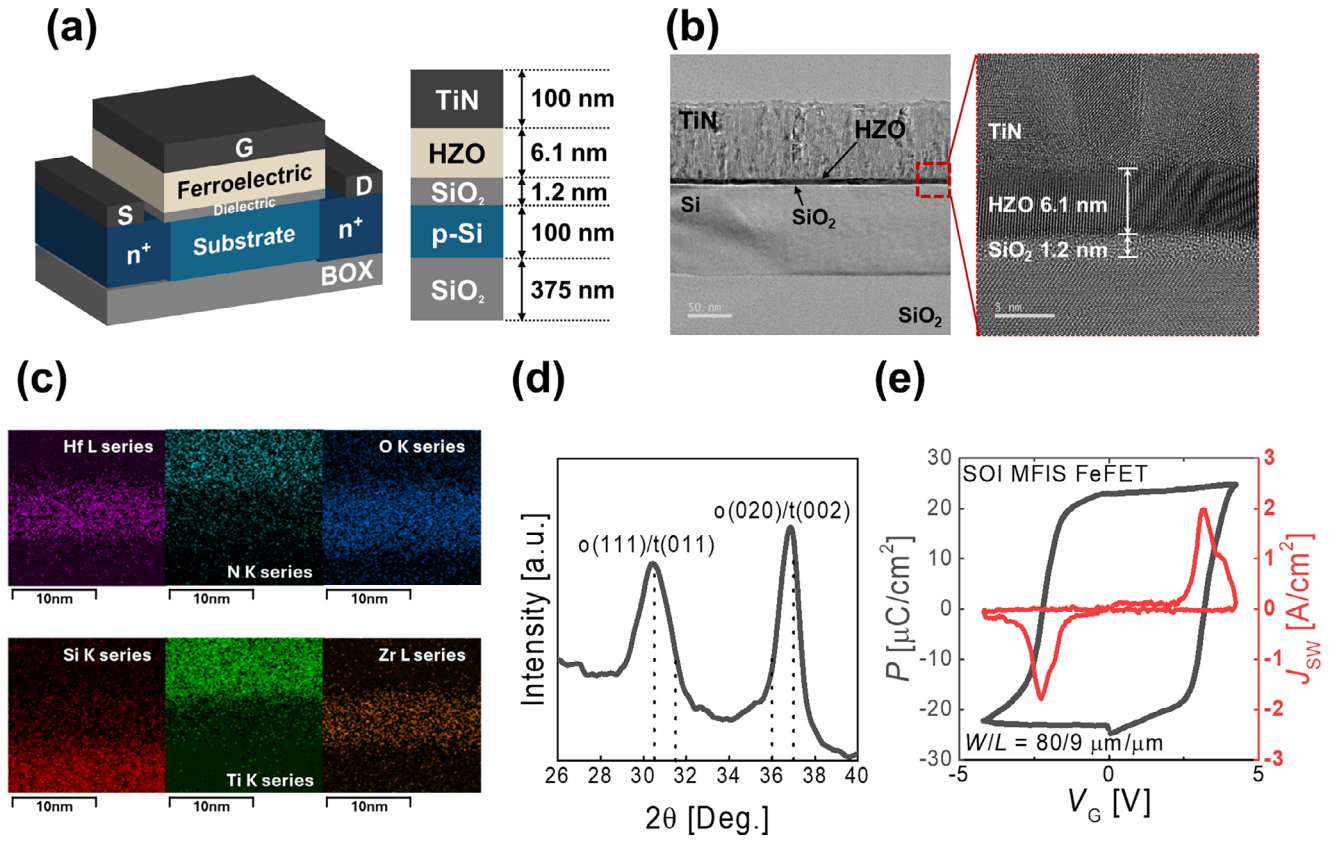

FIGURE 1 | Device structure and material characterization of the fabricated MFIS FeFET. (a) Schematic illustration of the MFIS FeFET structure, indicating the thickness of each layer. (b) Cross-sectional TEM images of the device and the magnified image of the TiN/HZO/SiO_2/Si gate stack. (c) EDS elemental mapping of Hf, Zr, Ti, Si, O, and N in the gate region. (d) GI-XRD pattern of the HZO film, indicating the formation of orthorhombic and tetragonal phases. (e) P–V_G and switching current characteristics of the fabricated FeFET.

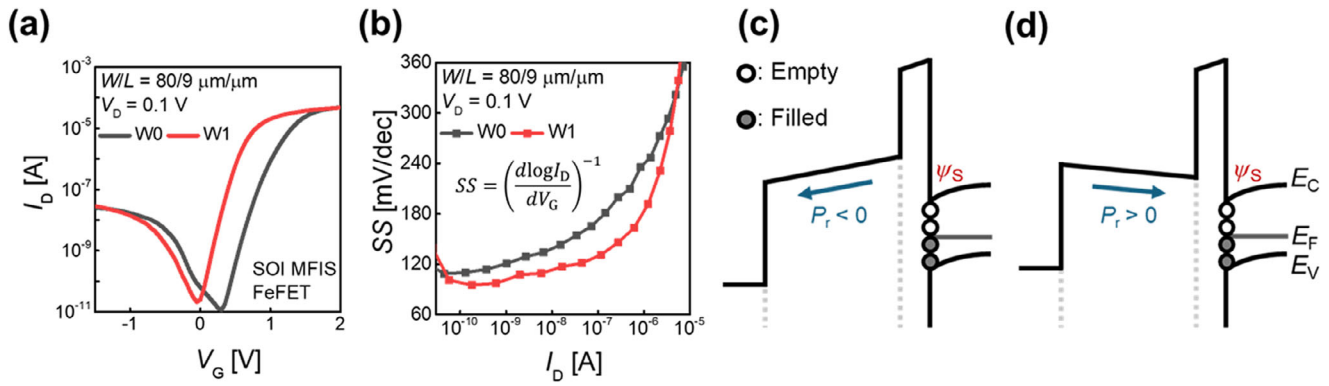

FIGURE 2 | (a) The transfer curves of the FeFET at W0 and W1 states, and (b) correlated SS-log(I_D) plot. Conceptual energy band diagrams at (c) W1 and (d) W0 states with the same I_D, or the same ψ_s, show the equivalent trap/de-trap configuration of the interface state.

However, despite being measured under identical electrical conditions and on the same device, the W0 and W1 states exhibited a clear difference in *SS* (Figure 2a,b). Within the conventional framework, such variation in *SS* would imply a change in the density or energetic distribution of interface states, possibly due to a different extent of trap interaction during the V_G sweep. However, in our measurements, no additional stress conditions (e.g., bias-temperature and/or cycling stress) were applied that could induce the creation or annihilation of interface states. Furthermore, since interface state distribution is typically modeled as a function of ψ_s, and given that the same drain current (I_D) implies identical ψ_s, it is inconsistent to attribute the observed *SS* variation to a change in C_{it} alone–distinct C_{it} values at the same ψ_s are physically implausible (Figure 2c,d).

Therefore, we consider that the difference in *SS* is not due to interface states, but rather results from altered trap dynamics within the gate insulator stack during the write operation [29–31]. Specifically, the polarization state of the ferroelectric HZO

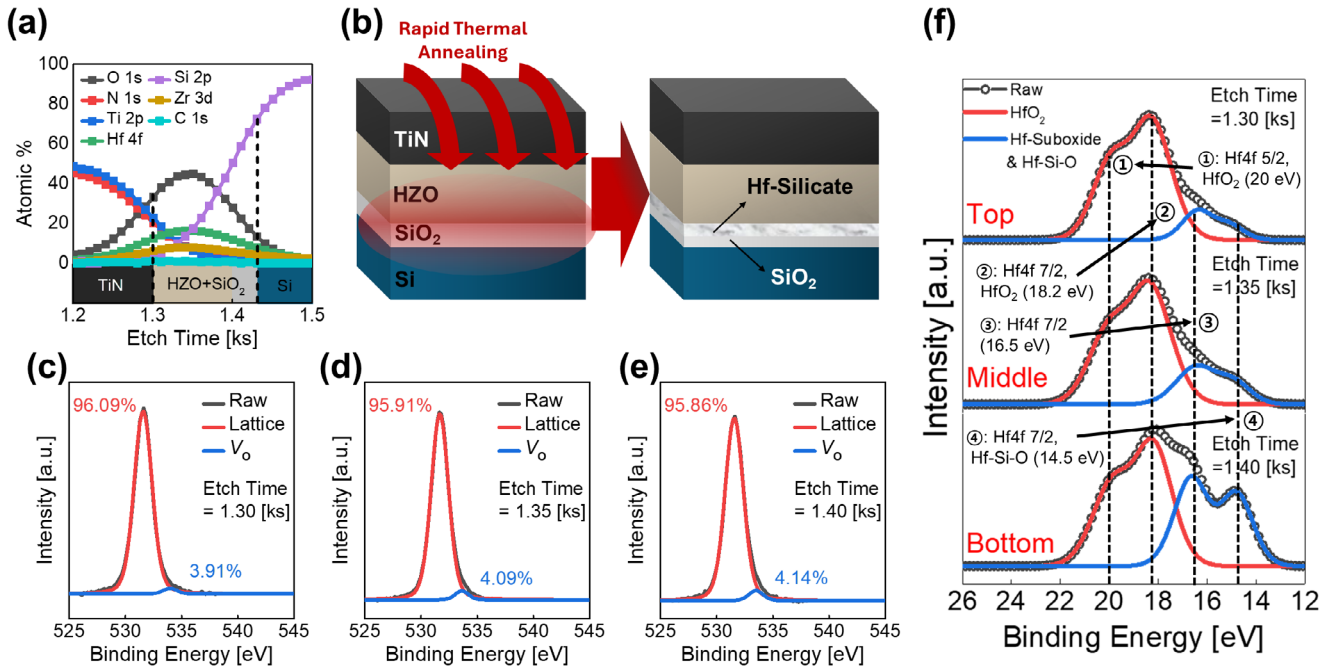

FIGURE 3 | (a) The XPS depth profile for TiN/HZO/SiO_2/Si. XPS spectra of the O 1s core level for HZO (b) near TiN gate (top), (c) bulk (middle), and (d) near HZO/SiO_2 interface (bottom). (e) A conceptual diagram of hafnium-silicate formation at the HZO/SiO_2 interface during the RTA process for HZO crystallization. (f) XPS spectra of Hf $4f_{7/2}$ and Hf $4f_{5/2}$ core corresponding to HZO near TiN gate (top), bulk (middle), and near HZO/SiO_2 interface (bottom).

layer differs between W0 and W1, which modulates the internal electric field distribution as shown in Figure 2c,d. This, in turn, affects the spatial and energetic distribution of trapped charges in pre-existing bulk or interfacial defects at the SiO_2/HZO interface, and their interaction with channel carriers. The altered field landscape leads to different trap response rates and effective trap densities during the *SS* measurement, resulting in the observed difference in slope.

Taken together, these findings suggest that interpreting *SS* variation purely in terms of static C_{it} distributions is insufficient. A more comprehensive model that considers the polarization-dependent potential profile and the time-dependent trapping dynamics provides a more consistent and physically grounded explanation for the *SS* behavior in FeFETs.

3.2 | Formation of Defect States at HZO/SiO_2 Interface and Remote Trap-Carrier Interaction

It is commonly known that the interface between materials contains more defect states than the bulk, considering that the dangling bonds, dislocations, and discontinuous atom arrangement. It is the reason why traditional trap density extraction techniques focus on the C_{it} at Si/SiO_2 interface. Therefore, we assume the most significant defect states in the gate stack exist at HZO/SiO_2 interfaces rather than SiO_2 and HZO bulk, as previously reported [32]. To investigate the physical origin of the defect states formed at the HZO/SiO_2 interface, X-ray Photoelectron Spectroscopy (XPS) depth profiling was performed across the gate stack of the fabricated MFIS device (Figure 3a). Full-range XPS depth profile of atomic percentage and corresponding EDS from Figure 1b are depicted in Figure S2.

The XPS analysis results in Figure 3c–e confirm that the oxygen-vacancy (V_O) sites created during rapid thermal annealing (RTA) are electrically active and readily capture or emit carriers. In the O 1s spectra, the lattice-oxygen component appears at a relatively low binding energy (BE), whereas the shoulder at relatively high BE is widely accepted as the signature of V_O-related oxygen deficiency [33–34]. Likewise, the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ doublet exhibits two distinct chemical states: the peaks at ~20 and 18 eV correspond to stoichiometric HfO_2, while the lower-binding-energy features at ~17 and 15 eV indicate the formation of an interfacial hafnium silicate ($HfSiO_x$) and other sub-oxides (Figure 3f) [35].

The spatial localization of these V_O sites at the HZO/SiO_2 interface is attributed to the interfacial $HfSiO_x$ layer that develops when the RTA temperature exceeds 400 °C–conditions intentionally employed to promote ferroelectric crystallization of HZO (Figure 3b). Earlier studies have shown that $HfSiO_x$ forms readily under thermal budgets, creating a trap-rich region that increases the local V_O density, distorts the electric field across the gate stack, and exacerbates gate leakage and threshold-voltage (V_T) instability [34, 36, 37]. The high-temperature anneal performed in this work for HZO crystallization affects the FeFET in the same manner, as evidenced by the pronounced Hf sub-oxide signal and the intensified V_O-related O 1s component. Collectively, the spectroscopic evidence confirms that the interfacial $HfSiO_x$–laden with V_O and sub-oxide species–acts as a highly defective layer whose electronic activity underlies the long-term charge-trapping behavior of our device.

Far from being a passive by-product, the V_O-rich $HfSiO_x$ layer functions as an electrically active, trap reservoir that markedly impairs gate control. Its high V_O density and favorable

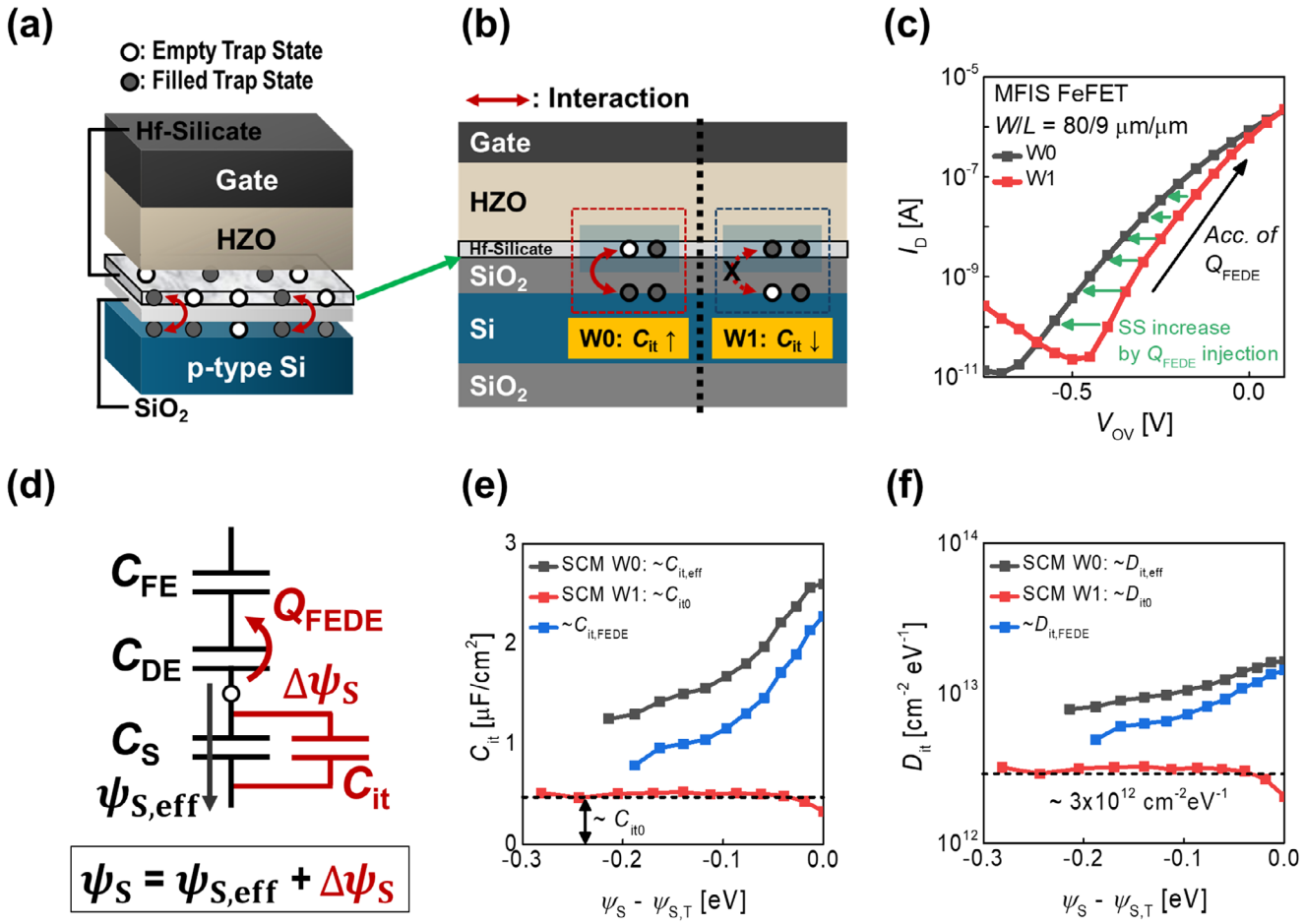

FIGURE 4 | (a) A conceptual diagram of remote trap-carrier interaction and its dependence on (b) W0 and W1 states. (c) Transfer curves plotted with V_{OV}. (d) An equivalent capacitor model of the MFIS capacitor with C_{it} and $Q_{FE/DE}$. (e) C_{it} and (f) D_{it} for W0 and W1 states with respect to $\psi_s - \psi_{s,T}$, where $\psi_{s,T}$ indicate ψ_s at $V_G = V_T$, are shown as separately extracted components.

spatial and/or energetic alignment with the tunneling path in SiO_2 make it the dominant contributor to *SS* change. Two remote trap-carrier interactions (RTCI) operate in tandem: (i) carriers in the Si channel tunnel through the SiO_2 and are directly captured (and later released) by $HfSiO_x$ defects–tunneling-related trapping (TRT); (ii) once charged, these defects electrostatically attract or repel channel carriers, driving additional carrier redistribution. The combined action of direct tunneling exchange and field-driven carrier redistribution weakens gate-to-channel coupling, thereby increasing both *SS* and *m*.

3.3 | Quantitative Analysis of Defect States from Subthreshold Operation Characteristics

The materials characterization results presented above already imply that the *SS* of MFIS FeFETs is governed by more than a static change in C_{it} at the Si/SiO_2 interface. Instead, an RTCI associated with defect states at the HZO/SiO_2 boundary, combined with time-dependent filling of tunneling-accessible traps, governs the observed behavior and SS degradation. As shown in Figure 4a, a trap-rich $HfSiO_x$ inevitably forms at the HZO/SiO_2 interface is particularly trap-rich; charge captured in this region screens the gate field and perturbs band bending in the Si channel, thereby distorting *SS* (Figure 4b). To quantify how these remote processes differentiate between the W0 and W1 states, we first applied the SCM. For a monotonic increase in trap population, the SCM predicts a corresponding monotonic rise in *SS*.

Figure 4c replots I_D vs. the overdrive voltage, $V_{OV} = V_G - V_T$, to emphasize the different *SS* of W0 and W1. The gentle slope in W0 than in W1 indicates that a larger number of slowly responding traps participate in the DC transfer curve, consistent with a weaker V_G-ψ_s coupling when polarization points toward the gate. Because intrinsic Si/SiO_2 interface states cannot be changed with polarization (Figure 2c,d); the variation must arise from remote HZO/SiO_2 interface traps. The effect of HZO/SiO_2 interface traps and trapped charge on the transfer curve can be explained by the capacitive coupling between HZO and SiO_2 with the model described in Figure 4d, which will be discussed later.

Applying SCM to the two transfer curves yields an effective C_{it} ($C_{it,eff}$)

$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_s + C_{it,eff}}{C_{ox}}\right) \quad (2)$$

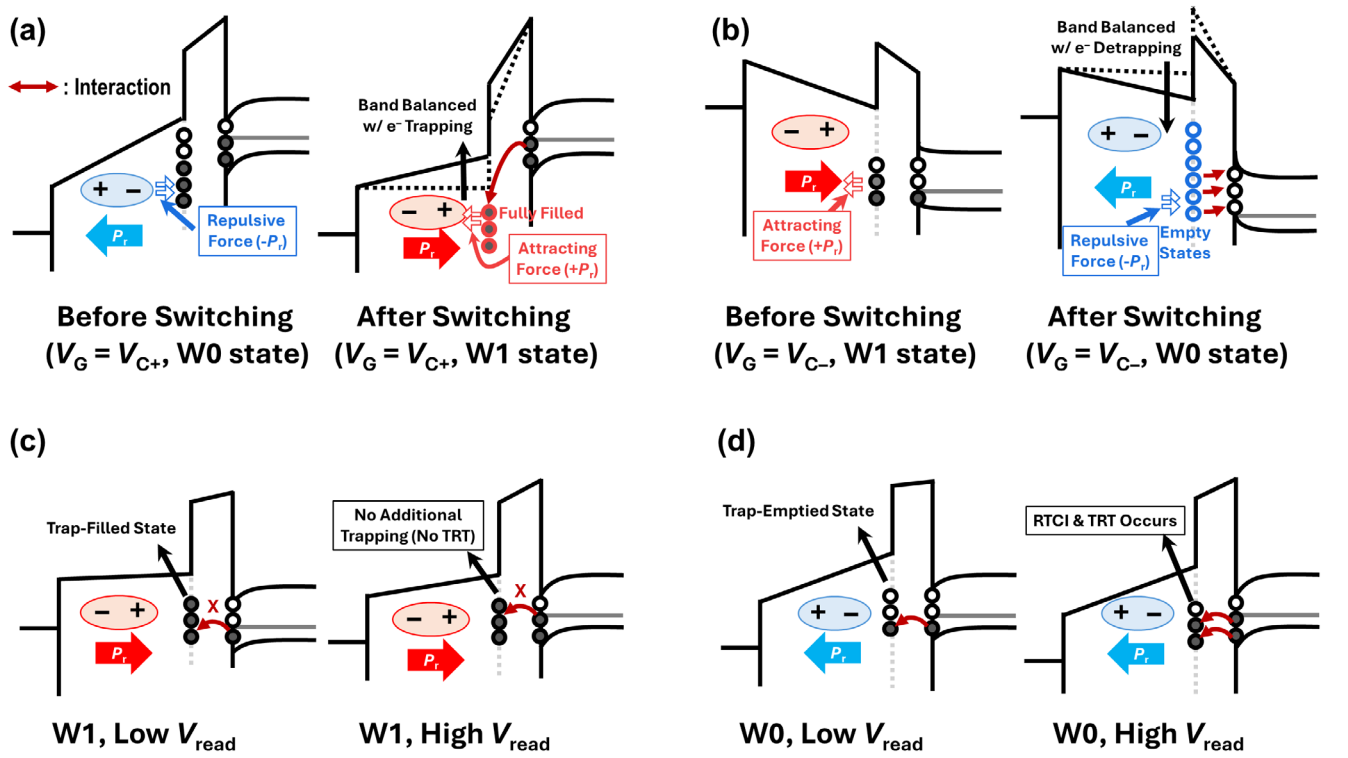

FIGURE 5 | Conceptual energy band diagram with polarization states and trap states. (a) Energy bands and defect states during W1 operation (V_G is a positive coercive voltage, V_{C+}), before and after polarization switching occurs. (b) Energy bands and defect states during W0 operation (V_G is a negative coercive voltage, V_{C-}), before and after polarization switching occurs. Corresponding energy band diagram and filled/emptied-defects with low/high V_{read} (c) at W1 and (d) at W0.

and

$$C_{it,eff} = C_{it0} + C_{it,FE/DE} \tag{3}$$

where C_{it0} originates from Si/SiO_2 interface states and $C_{it,FE/DE}$ projects the HZO/SiO_2 remote traps onto the Si surface. Equation (3) is equivalent to differentiating the stored charge density with respect to the surface potential, which is

$$\frac{dQ_{it,eff}}{d\psi_s} = \frac{dQ_{it0}}{d\psi_s} + \frac{dQ_{it,FE/DE}}{d\psi_s} \tag{4}$$

and

$$C_{it,eff}(\psi_s) = \frac{dQ_{it,eff}}{d\psi_s} = q^2 D_{it,eff} \tag{5}$$

The extracted values (Figure 4e,f) differ markedly–$D_{it,eff}$ is ~4×10^{12} $cm^{-2}eV^{-1}$ in W1 and larger than ~7.8×10^{12} $cm^{-2}eV^{-1}$ in W0–directly corroborating the RTCI/TRT hypothesis. It is noteworthy that C_{it0} (Q_{it0}) should be invariant between W1 and W0 at any given I_D; the entire SS change is ascribable to $C_{it,FE/DE}$. Hence, the larger $C_{it,eff}$ observed in W0 than in W1 reflects an enhanced tunneling probability and/or trapping for carriers interacting with HZO/SiO_2 interface states in W0 states.

Figure 5 schematically depicts the energy band diagram during W1 and W0 operation. A positive V_G pulse drives the polarization downward, lowers the SiO_2 tunneling barrier by an additional electric field, and rapidly fills and saturates $HfSiO_x$ traps (Figure 5a). Conversely, a negative V_G pulse flips the polarization, empties the traps or promotes hole capture (Figure 5b), and leaves the HZO/SiO_2 interface largely unoccupied at the start of the subsequent V_G sweep.

The V_G sweep in W1 state begins with a trap-saturated $HfSiO_x$; additional trapping is energetically disfavored, rendering $C_{it,FE/DE}$ negligible (Figure 5c). Conversely, with empty $HfSiO_x$ traps in W0 state, injected electrons during a V_G sweep are readily captured; incremental V_G therefore builds $Q_{FE/DE}$ rather than increasing channel inversion (Figure 5d). The attendant loss of ψ_s yields a larger SS and m. Consequently $C_{it,eff} \approx C_{it0}$ in W1 state. Hence, the difference $\Delta C_{it,eff} = C_{it,eff}(W0) - C_{it,eff}(W1)$ quantitatively gauges RTCI strength.

The $\Delta C_{it,eff}$, which is directly related to $D_{it,FE/DE}$, can be converted to $D_{FE/DE}$ by considering capacitive coupling between HZO and SiO_2 (Figure 4d). Assuming identical ψ_s in both states, the flat-band voltage shift (ΔV_{FB}) induced by the actual trap charges at the two interfaces satisfies

$$\begin{aligned} \Delta V_{FB}^{(Si/SiO_2)} &= -\frac{\Delta Q_{it}(\psi_s)}{C_{ox}} \\ \Delta V_{FB}^{(HZO/SiO_2)} &= -\frac{\Delta Q_{FE/DE}(\psi_s)}{C_{FE}} \end{aligned} \tag{6}$$

where $C_{ox} = C_{FE} || C_{DE}$. Considering that $Q_{it,FE/DE}$ affects an equivalent effect on ΔV_{FB} with $Q_{FE/DE}$, then the two equations are

equivalent, then,

$$\frac{\Delta Q_{FE/DE}(\psi_s)}{\Delta Q_{it,FE/DE}(\psi_s)} = \frac{D_{FE/DE}(\psi_s)}{D_{it,FE/DE}(\psi_s)} = \frac{C_{FE}}{C_{ox}} = \frac{C_{FE}+C_{DE}}{C_{DE}} \quad (7)$$

Note that defect density (D) is equivalent to energy derivative of Q. With C_{FE} = 4.4 μF/cm^2 and C_{DE} = 2.9 μF/cm^2, calculated from the device size in Figure 1a,b, the geometric factor is $(C_{FE}+C_{DE})/C_{DE} \approx 2.5$. Therefore, the measured $\Delta D_{it,eff} = D_{it,FE/DE}$ in (Figure 4f) converts to $D_{FE/DE} \approx 2.5\times D_{it,FE/DE} = 1 \times 10^{13}$ cm^{-2}eV^{-1}, roughly two times the intrinsic Si/SiO$_2$ density, D_{it0}. These quantitative results confirm that the V_O-rich HfSiO$_x$ layer significantly contributes the RTCI-driven degradation in *SS* and *m* depending on polarization states. Mitigation strategies must therefore target (i) suppressing defect states in HfSiO$_x$ by passivating V_O sites, (ii) suppressing TRT by a robust dielectric, and/or (iii) engineering the capacitive stack (e.g., increasing C_{DE}) to weaken the effect of $D_{FE/DE}$ as explained in Equation (7). Note that the projection factor introduced in Equation (7) is a purely electrostatic (geometric) quantity determined by the capacitances of the FE and DE layers (i.e., by their dielectric constants and physical thicknesses). As such, the projection factor is a structural parameter of the gate insulator stack and is not itself modified by band-bending or polarization state. For the present stack (HZO 6.1 nm / SiO$_2$ 1.2 nm) projection factor evaluates to ≈ 2.5; however, it will change for different dielectric constants or layer thicknesses and therefore must be recalculated for other device geometries.

It is important to distinguish this structural projection from the state-dependent traps that are electrically active in a given measurement. In our analysis, we adopt the practical assumption that "equal I_D corresponds to equal Si surface potential ψ_S"; under this condition, the extracted C_{it} (and hence the deduced D_{it}) represents the aggregate electrical contribution of traps that respond at that ψ_S. Thus, while the projection factor itself is unchanged between W0 and W1, the subset of traps probed (determined by trap energy distribution and capture/emission time constants) depends on the poling state because W0 and W1 produce different band-bending and hence different trap occupancies. In other words, apparent differences in the converted trap density between W0 and W1 can arise from occupancy and kinetic effects even when the underlying structural projection factor remains constant.

In other words, D_{it} values can be numerically similar between HZO/SiO$_2$ and Si/SiO$_2$ interfaces, yet device-level metrics such as memory window and V_T stability differ markedly: device performance is governed not only by the trap density but critically by the time constants, and spatial proximity to the channel. Traps that are energetically shallow, closer to the semiconductor, or possess capture/emission kinetics that match programming/retention time scales will disproportionately affect retention, endurance, and V_T shifts even if the total D_{it} is comparable.

3.4 | Capacitance-Resolved Defect Metrology and Cross-Validation with SCM

Building on the DC I_D–V_G analysis in the previous section, we confirmed that the *SS* disparity between W0 and W1 originates not only from intrinsic Si/SiO$_2$ interface traps but also from remote traps at the HZO/SiO$_2$ interface. Yet, as schematically indicated in Figure 6a, SCM derives from quasi-static I_D-V_G data and therefore blends the electrical responses of traps having different spatial locations and time constants. To deconvolve these contributions and cross-validate SCM, we adopted two capacitance-based techniques (Figure 6b): (i) Multi-Frequency C_{gds}-V_G (MFCV) and Terman Method (TM).

The gate to drain/source capacitance (C_{gds}) spectra were measured from 1 kHz to 1 MHz (Figure 6c–e) with sweeping the DC gate bias with a small signal added ($V_g = V_G + v_g$). Fast traps can respond even at 1 MHz but are gradually suppressed as frequency increases, whereas slow traps respond only at low frequency (~ 1 kHz). However, considering the lowest frequency in this work was 1 kHz, which is not low enough for RTCI to occur [38], the frequency dispersion in C_{gds} could be caused by the defect states at SiO$_2$/Si interface and near-border–or D_{it0}.

Then, the small-signal equivalent capacitance is $C_{LF} = C_{ox}||(C_s+C_{it0})$ and $C_{HF} = C_{ox}||C_s$ gives

$$C_{it0} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} = q^2 D_{it0} \quad (8)$$

To complement MFCV, we extract the $C_{it,eff}$ at 1 MHz by TM. TM converts the V_g shift (ΔV_g) to obtain the same C_{gds} between a measured high-frequency C_{gds}-V_g trace and an ideal MOS C-V curve into C_{it} via

$$C_{it} = C_{ox}\left|\frac{dV_G}{d\psi_s}\right|\Delta V_G(\psi_s) \quad (9)$$

Because the W1 state already embodies a trap-saturated HZO/SiO$_2$ interface (Figure 5c), 1 MHz C_{gds}-V_G curve in W1 state was adopted as the reference; any additional ΔV_G in W0 is thereby attributed to $C_{it,FE/DE}$ (Figure 5d). Figure 6f reveals a clear slope divergence between W0 and W1–even at 1 MHz where small-signal trapping is nominally frozen. This large-signal effect arises as the Fermi level (E_F) sweeps through the band gap, refilling traps below E_F, mirroring the SCM.

In detail, as shown in Figure S4, the Terman method can also be performed using *C*–*V* curves measured at low frequencies, yielding a nearly identical D_{it}. However, to ensure a clearer and more consistent assumption, we conducted the analysis using high-frequency *C*–*V* data.

Quantitatively, TM yields $D_{it,FE/DE} \approx 4\times10^{12}$ cm^{-2}eV^{-1}, values that align to within 15 % of the SCM value, demonstrating that TM is sufficiently sensitive to the polarization-induced occupancy change of remote traps (Figure 6g–h).

4 | Conclusion

We have demonstrated that the polarization-dependent characteristics of MFIS FeFETs stem from a dual-interface defect landscape comprising intrinsic Si/SiO$_2$ traps (D_{it0}) and remote HZO/SiO$_2$ traps ($D_{FE/DE}$). By combining SCM, MFCV, and TM,

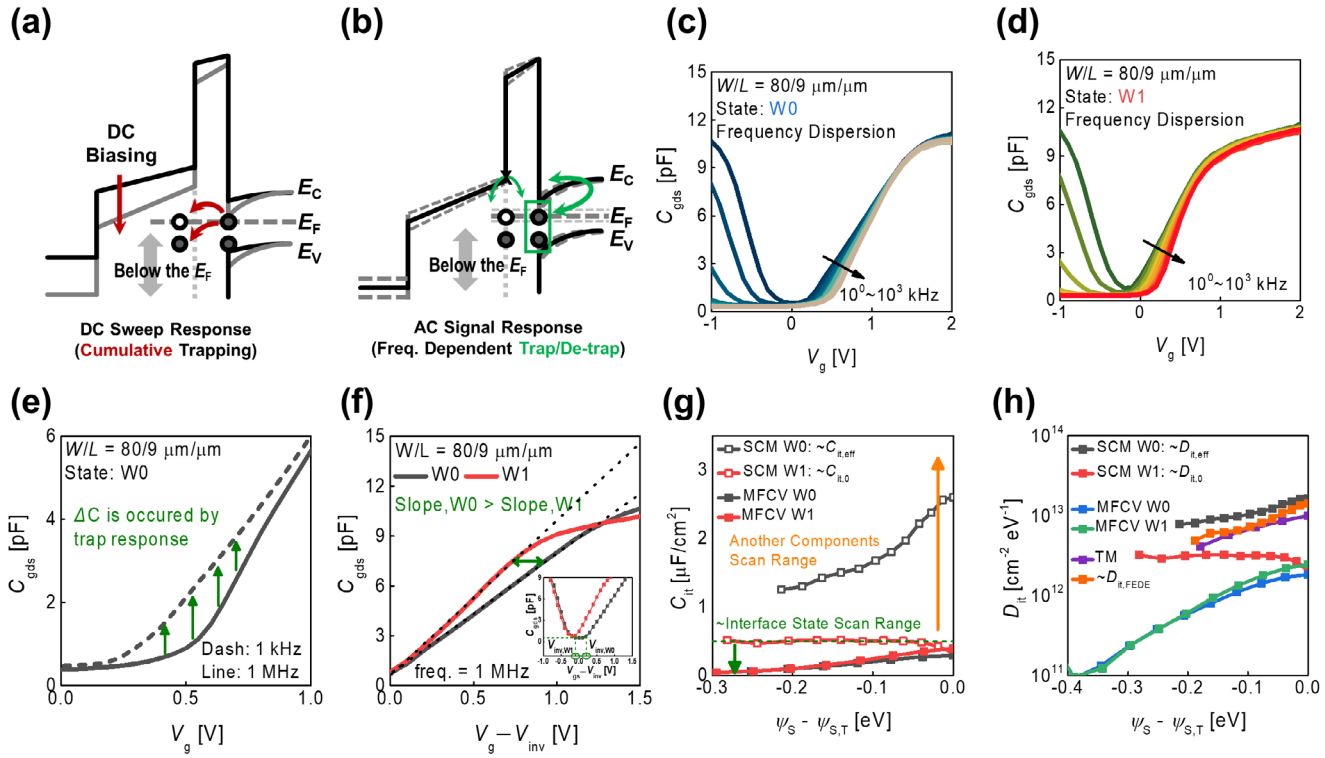

FIGURE 6 | (a) Conceptual energy band diagram for explaining the difference in remote trap response with (a) DC V_G sweep and (b) AC small-signal gate bias (v_g), which stands for SCM/TM and MFCV. C_{gds}-V_g curves with various frequencies of the MFIS FeFET in (c) W0 and (d) W1 states. (e) Frequency dispersion in C_{gds} caused by the difference in defect states that can react at different frequencies, and (f) ΔV_g caused by DC V_G biasing and tunneling-related charge trapping during C_{gds}-V_g sweep. (g) $C_{it,eff,}$ and (h) $D_{it,eff}$ plot for comparing the SCM and *C-V* based methods.

we quantitatively separated and cross-validated the two interface-state densities–$D_{it0} \approx 4 \times 10^{12}$ and $D_{it,FE/DE} \approx 4 \times 10^{12}$ $cm^{-2}eV^{-1}$ (equivalent to $D_{FE/DE} \approx 1 \times 10^{13}$ $cm^{-2}eV^{-1}$). In addition, the capacitive coupling analysis Equation (7) revealed a geometric projection factor of ≈ 2.5, confirming that the effect of the remote traps (defect states in the V_O-rich $HfSiO_x$ layer) is suppressed by the geometric projection factor. These insights furnish a quantitative metrology for assessing HZO/SiO_2 quality–one of the key levers for further FeFET performance improvements in terms of memory window, V_T stability, SS, and read-after-write latency (RWL). The methodology is broadly applicable to other FeFETs where remote trap-carrier interactions (RTCI) govern reliability.

Author Contributions

The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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